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January 29–30, 2025

Delta-L Measurement Analysis: Extending PCB Trace Insertion Loss Measurements to 67 GHz

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Contributors

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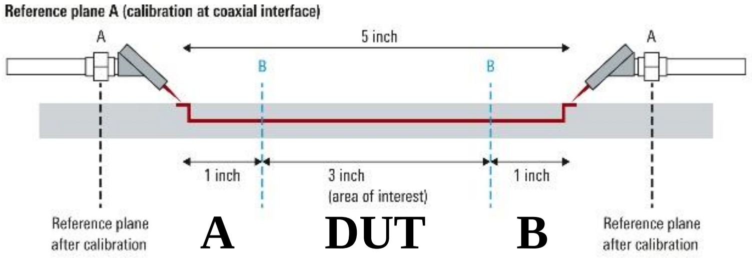
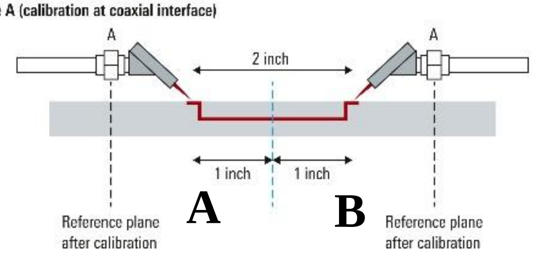
- Richard Zai – PacketMicro
- Giorgi Tsintsadze – Missouri S&T EMC Laboratory (now at Cisco)
- John Cheng – PacketMicro

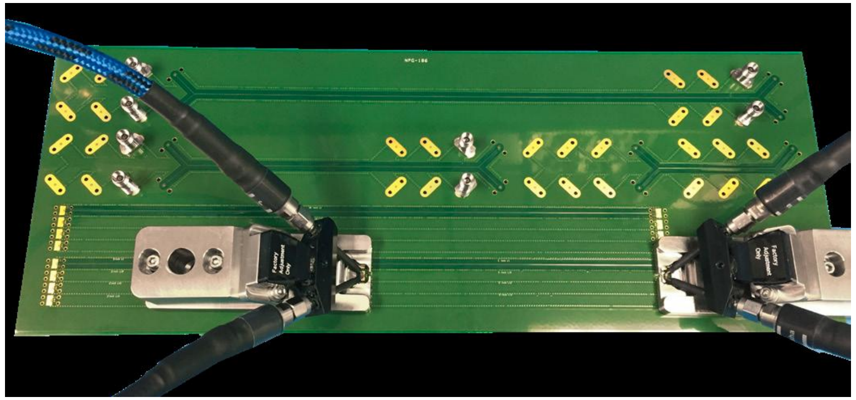
Delta-L 4.0 Methodology – to 40 GHz

2”, 5”, 10” trace lengths used for IL extraction

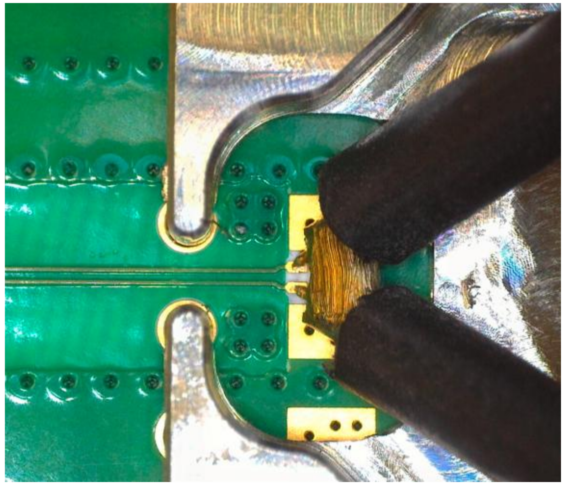




Test Vehicle with PacketMicro Probes and Bases



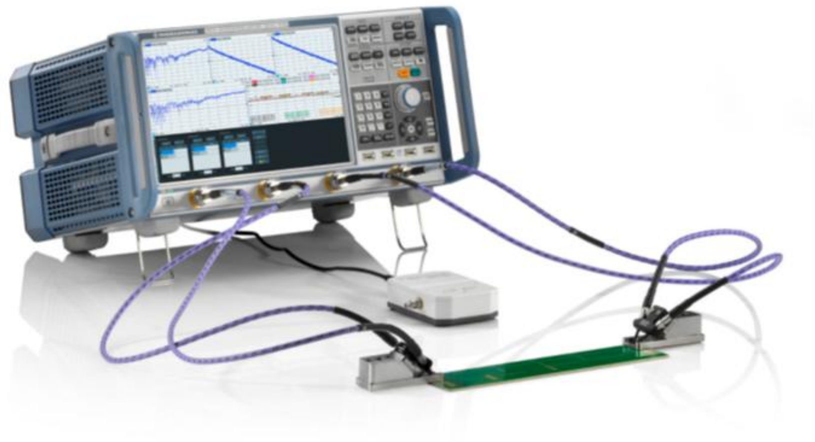
Universal Probe Launch with PacketMicro Probes



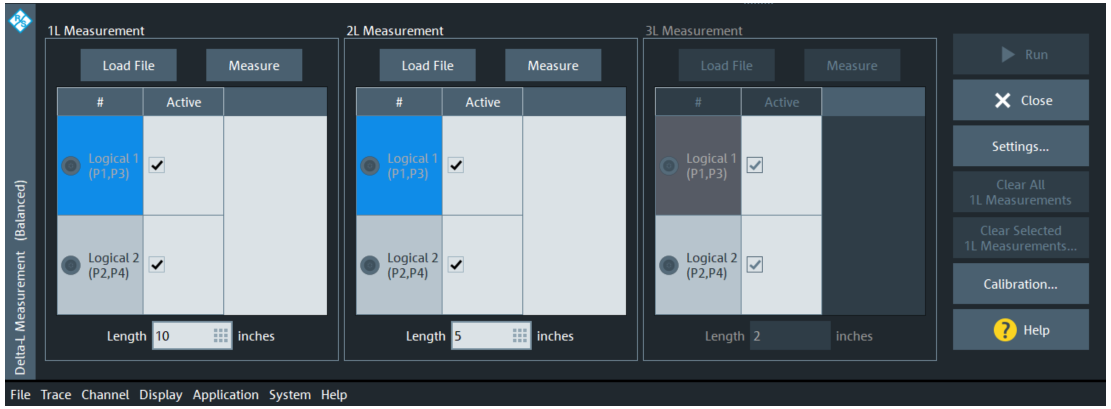
Use eigenvalue extraction method to get $\gamma=\alpha+j\beta$ for DUT, and IL in dB/inch

Workflow Implemented in Commercial Toolsets

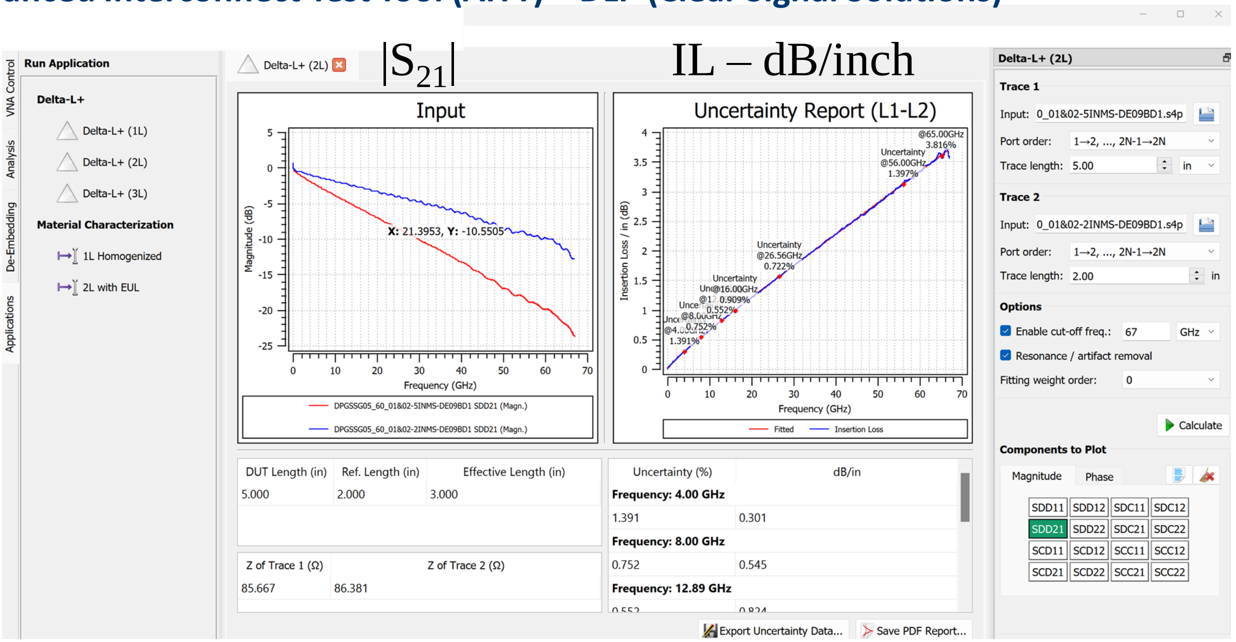
R&S®ZNB40 setup with Delta-L 4.0 probes



Delta-L Workflow for 2L on R&S®ZNB40



Advanced Interconnect Test Tool (AITT) – DLP (Clear Signal Solutions)

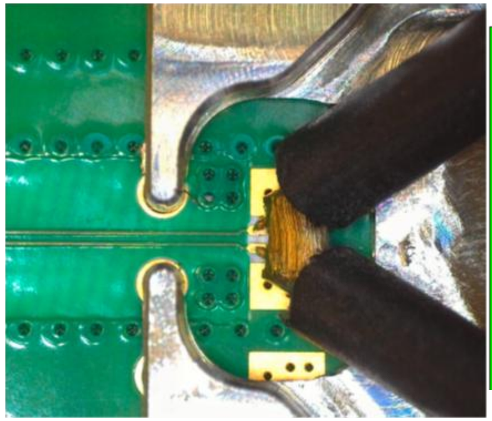


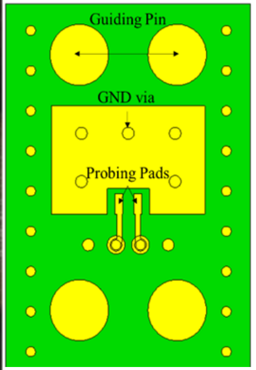
Next Step – Delta-L to 67 GHz

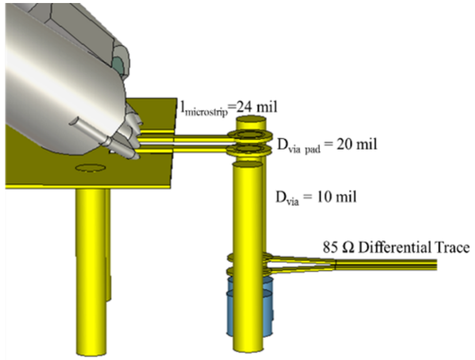
- Want to achieve 56 GHz over 1 lane for 224 Gbps data rate/PAM4, PCIE gen 7 128 GT/s over 1 lane
- Need to achieve 67 GHz for Delta-L method
  - using hand-held probes for use in large-volume measurements and in fabrication environment
  - Must have a universal footprint to accommodate handheld probes and rapid alignment/placement
  - 0.4 mm most likely a minimum probe pitch for rapid alignment due to manufacturing tolerance in PCB fab
- Must have trace pattern lengths for Delta-L to meet IEEE 370 STD for de-embedding accuracy – e.g., 1” & 4”, 2” & 5”?

Delta-L 4.0 (to 40 GHz) Solution

Universal Probe Launch with PacketMicro Probes

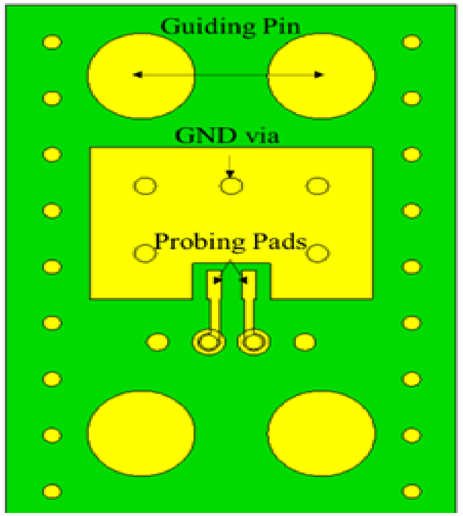


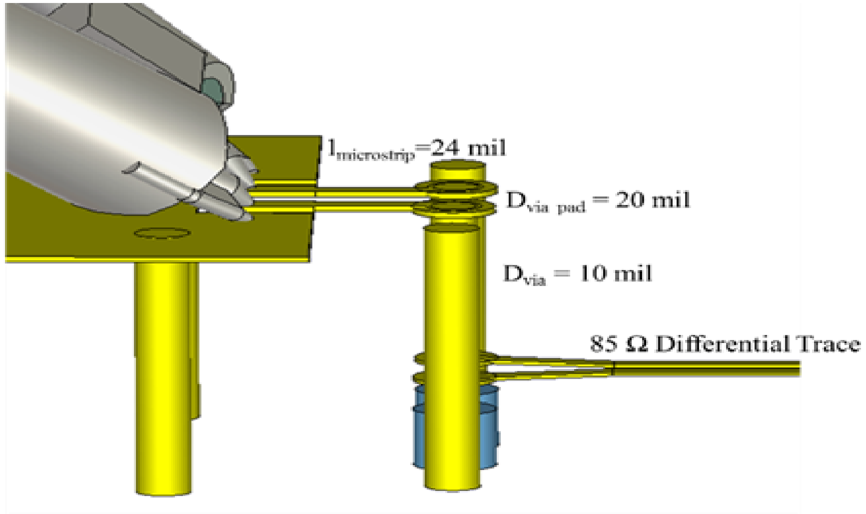


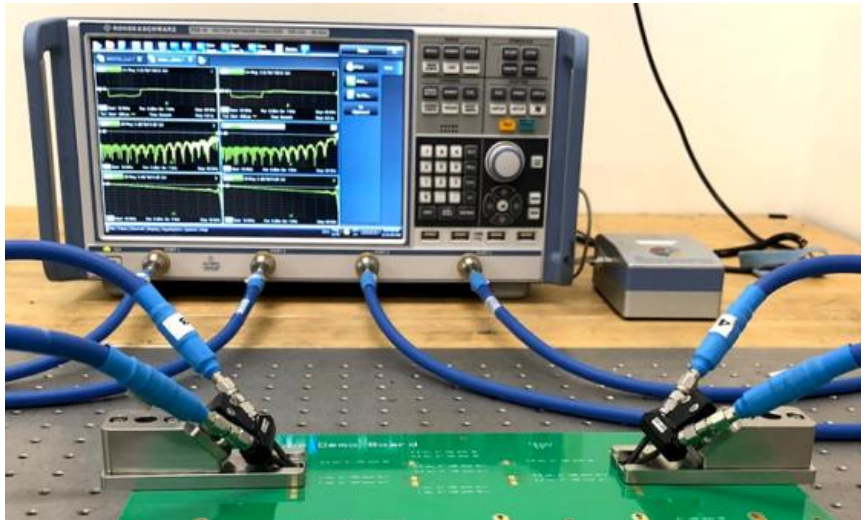


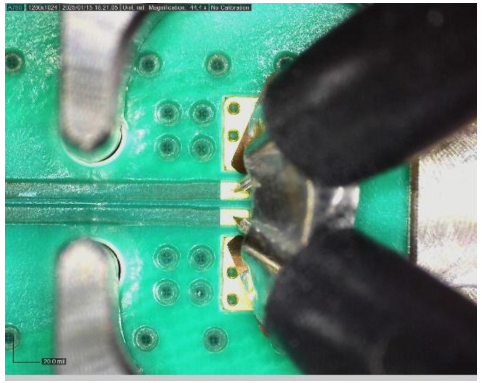
Probing Solution to 67 GHz

- Optimize probe and via transition simultaneously to achieve a RL>6dB at 67 GHZ
- Achieve an IL < 6 dB at 67 GHz by using shorter 2X Thru









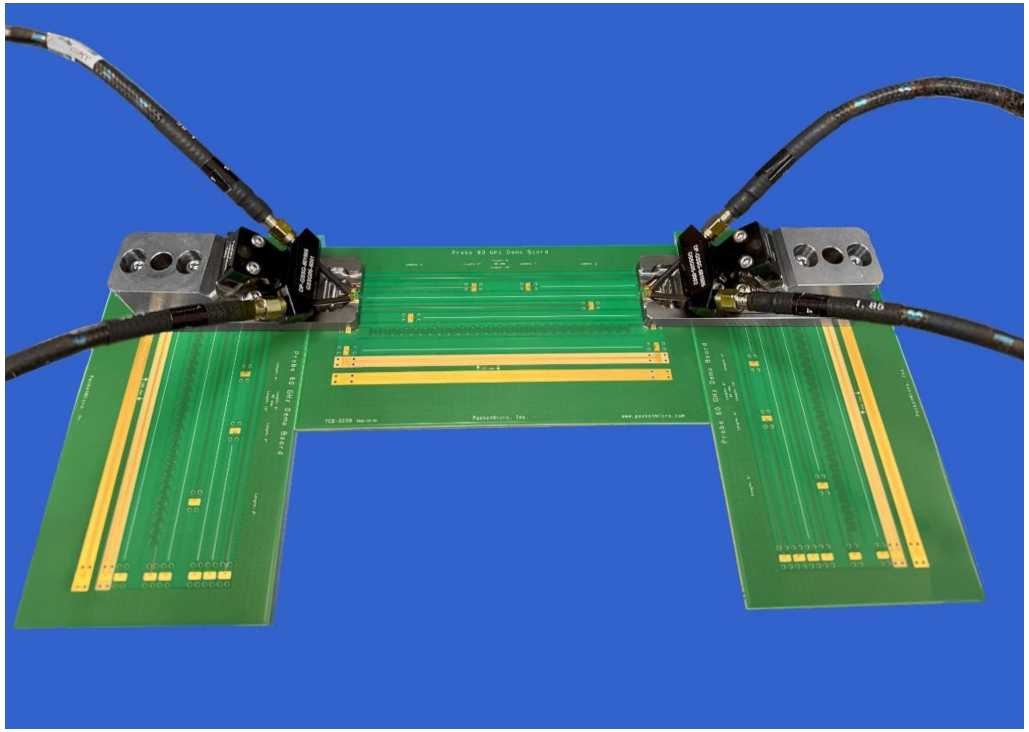
PacketMicro
GSSG probe

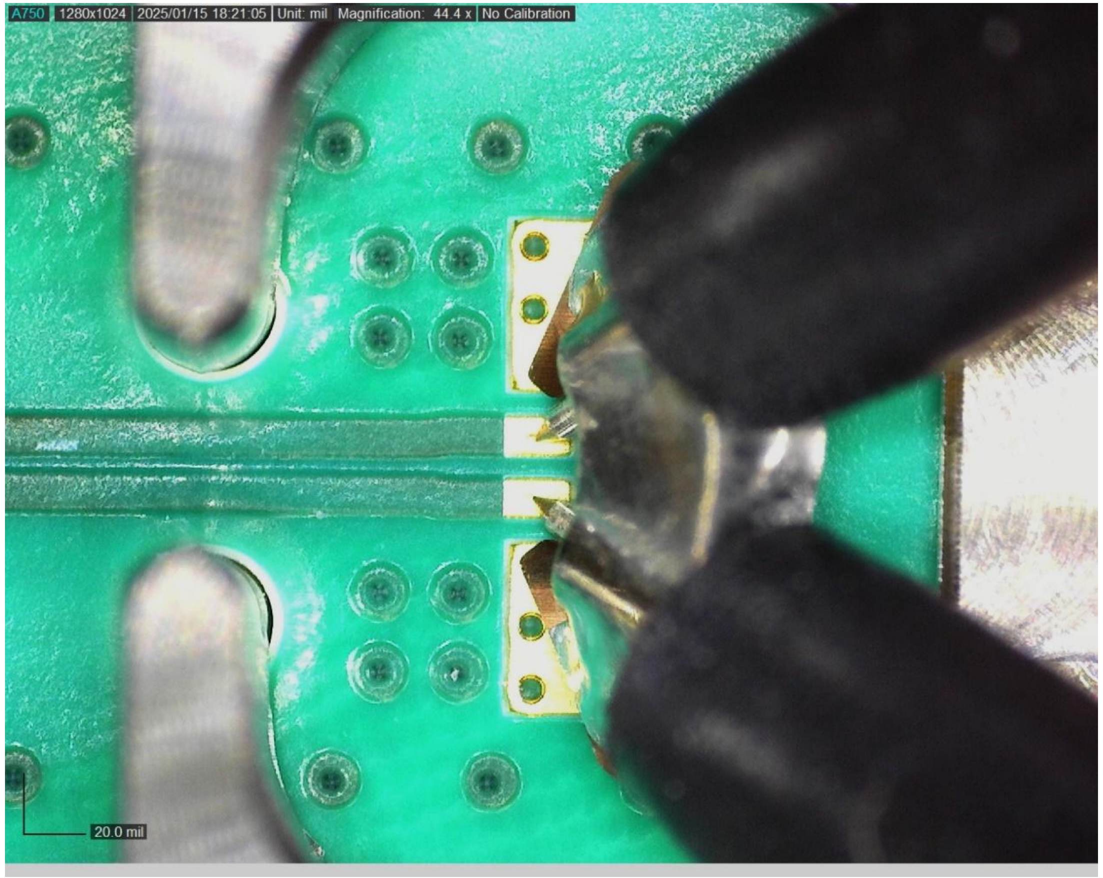
Booth 1155

Status – PacketMicro Probes

Probe properties:

- 0.5 mm pitch
- GSSG configuration
- 3-mil robust probe tips
- 47-mil Coaxial cable
- 1.85mm Samtec connector
- Stainless base

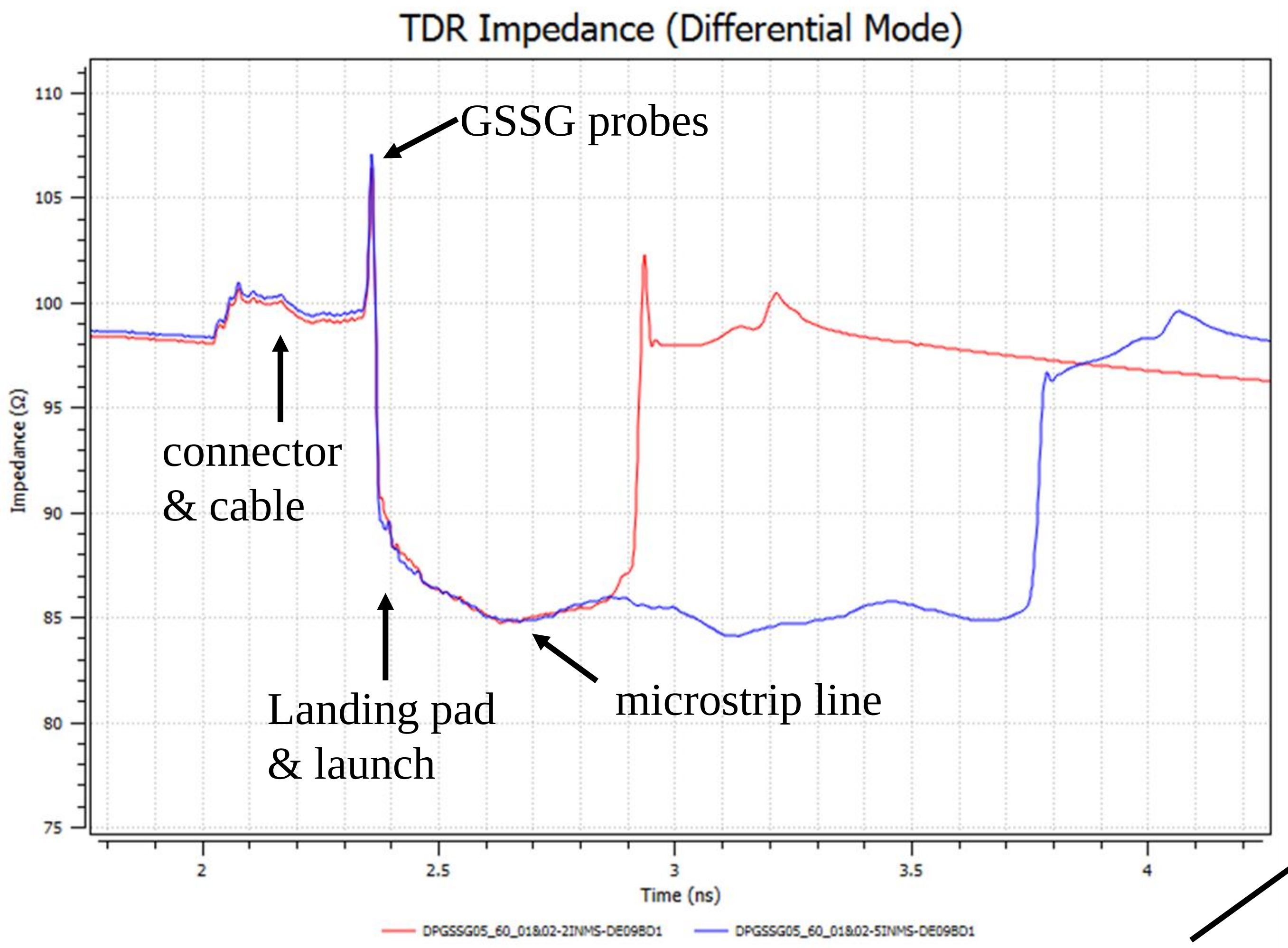


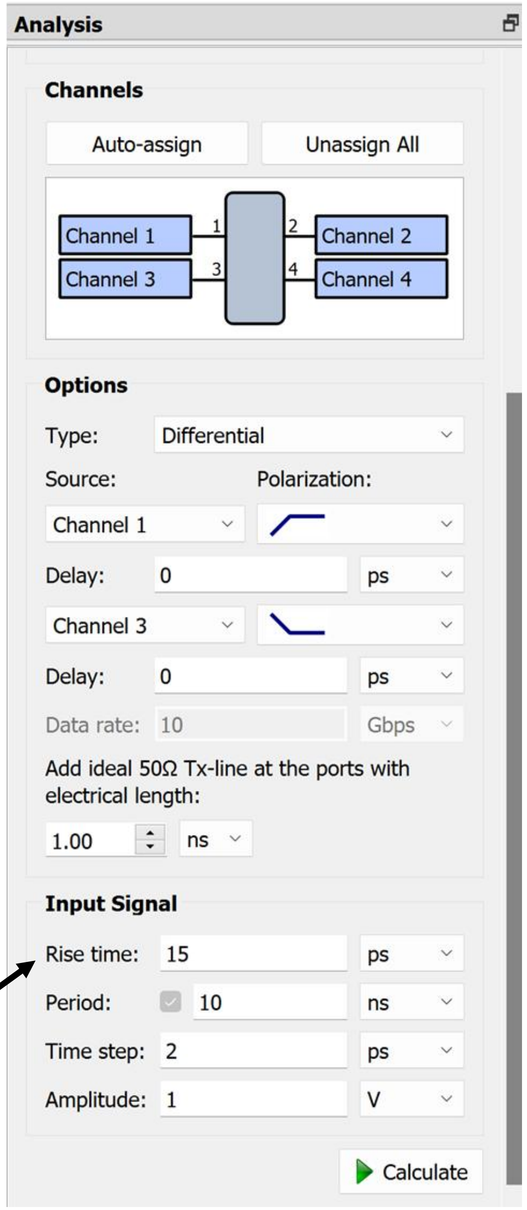


PacketMicro
GSSG probe

Booth 1155

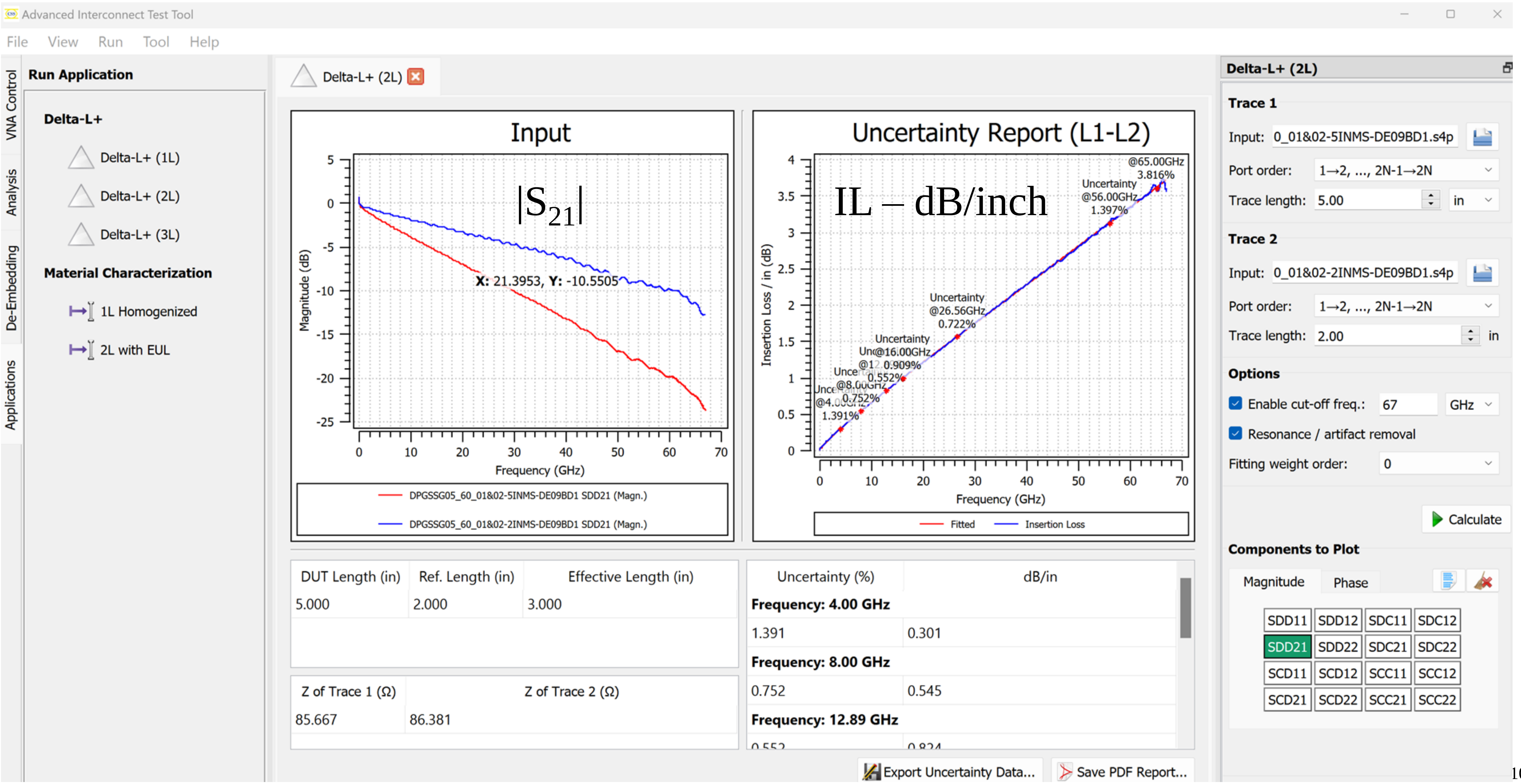
Status – 67 GHz GSSG Probes on Microstrip - TDR



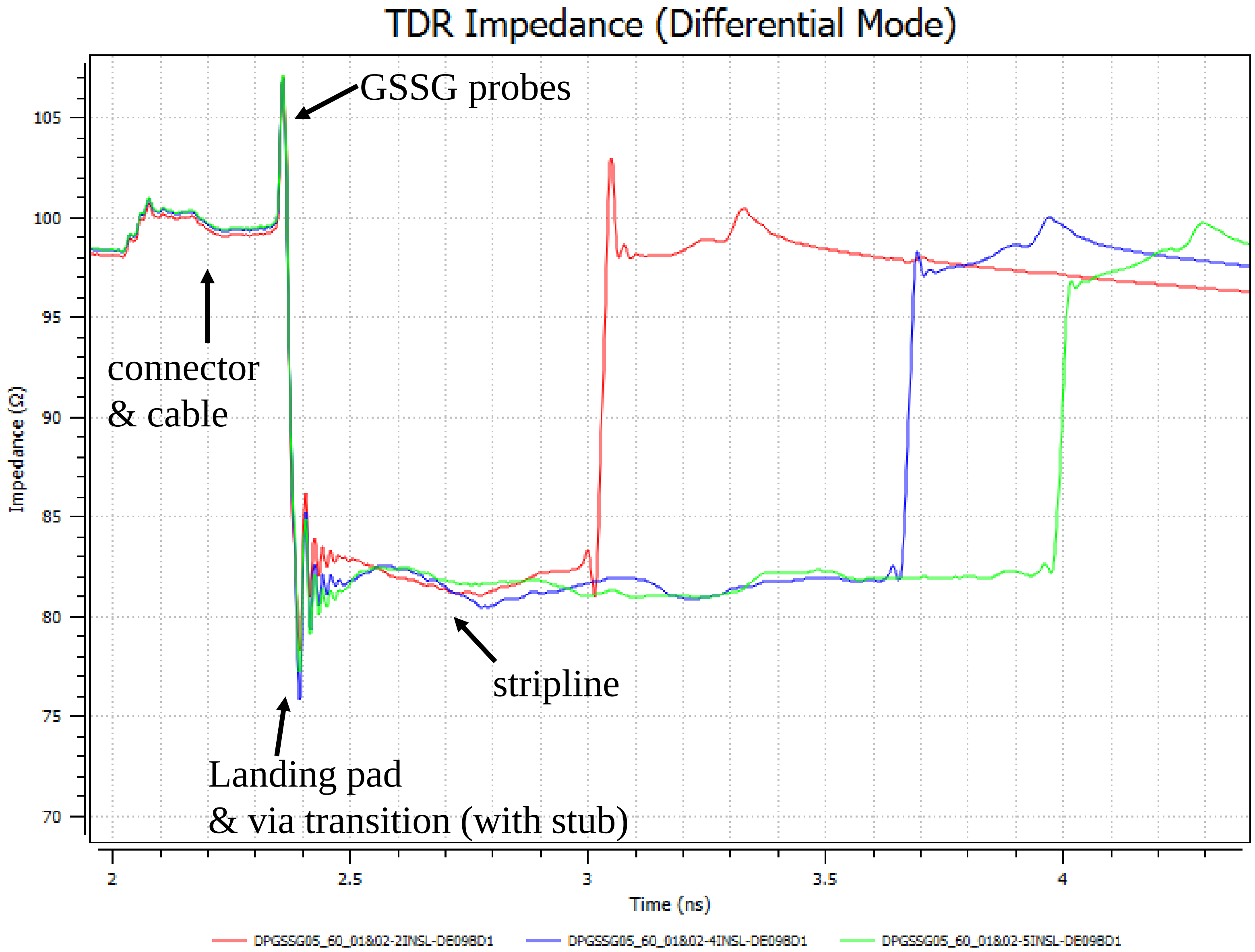


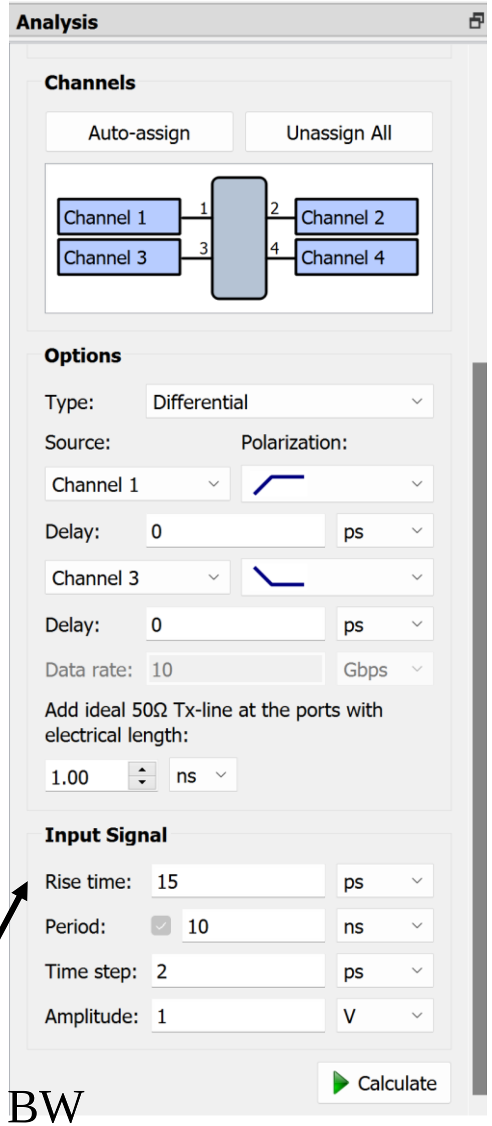
67 GHz BW

Status – 67 GHz GSSG Probes on Microstrip – Delta-L



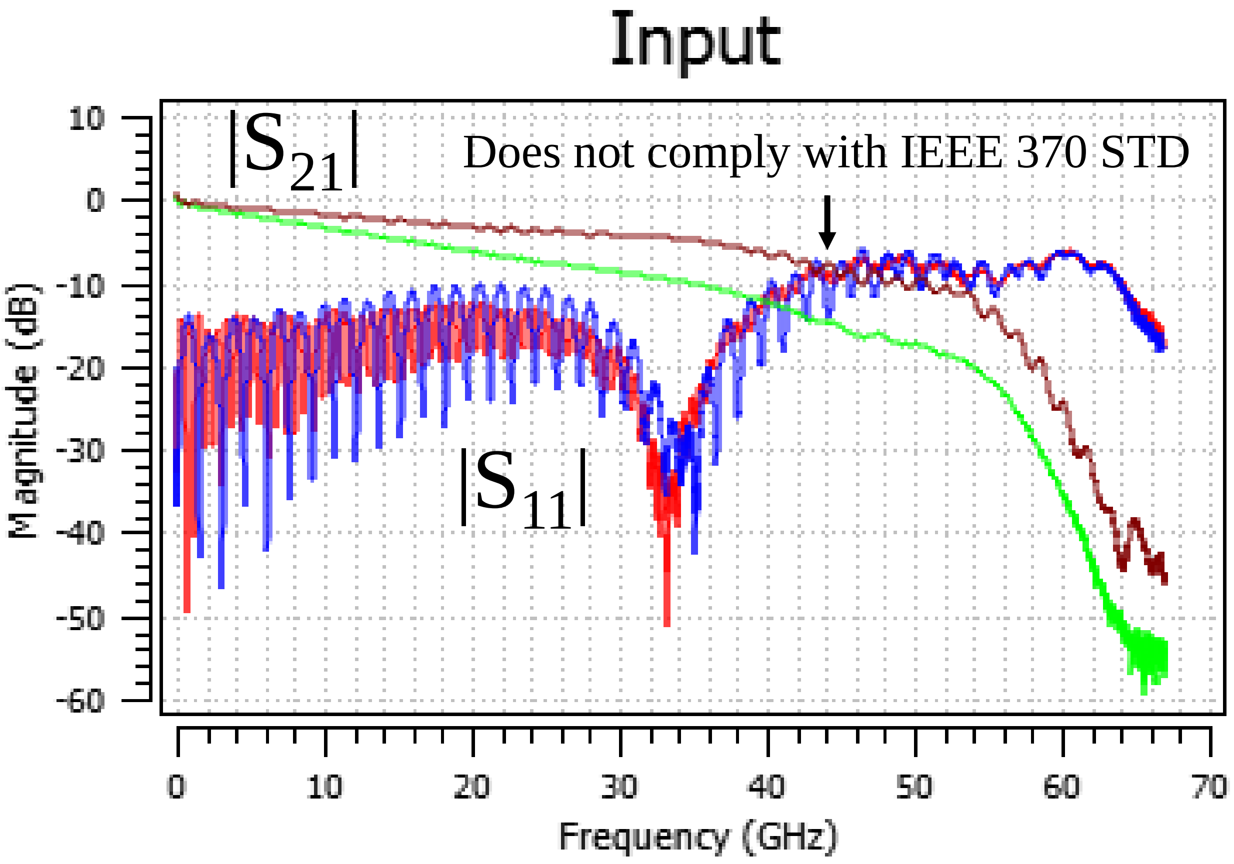
Status – 67 GHz GSSG Probes on Stripline – TDR

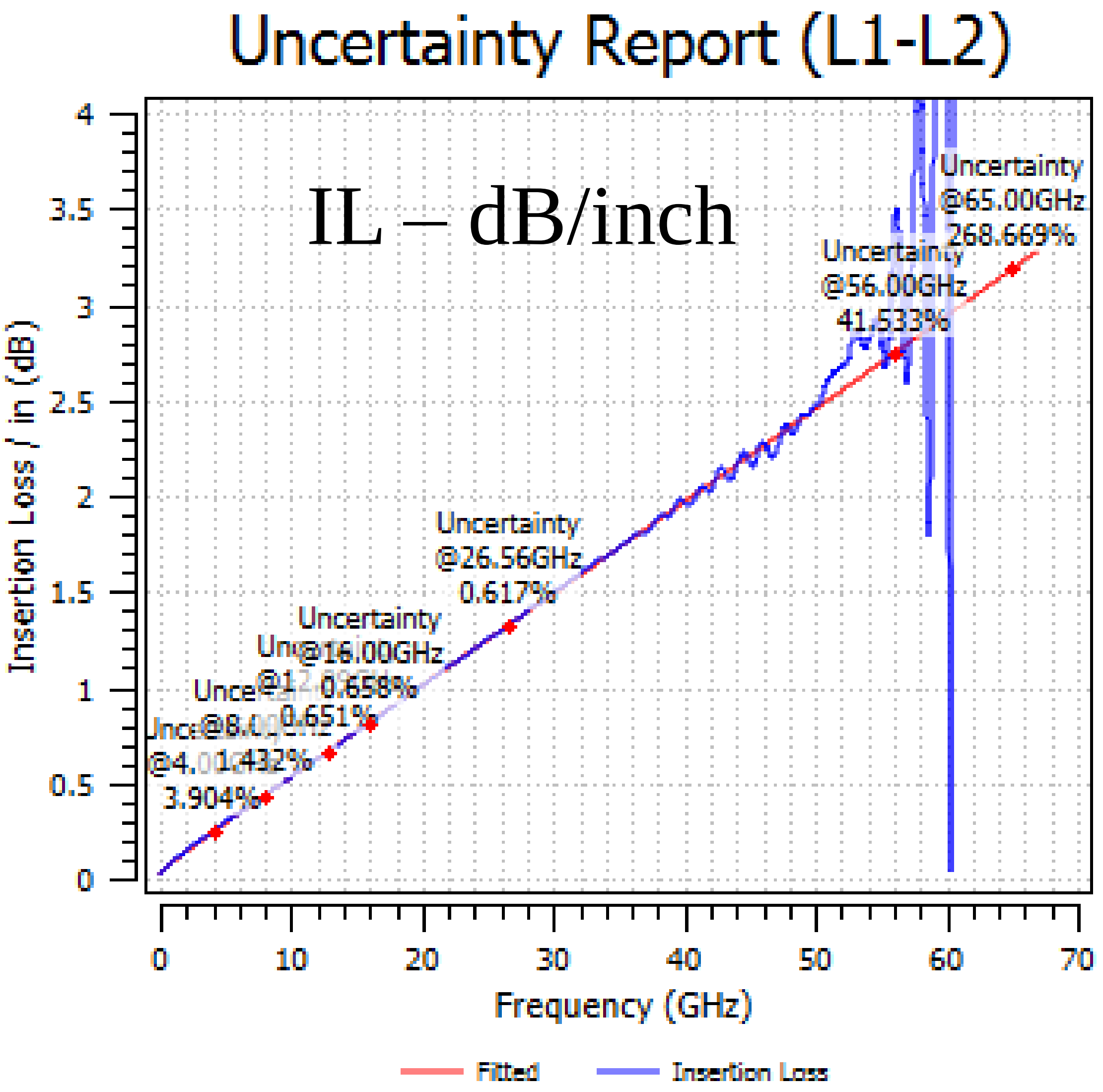




67 GHz BW

Status – 67 GHz GSSG Probes on Stripline – Delta-L





- RL and IL for 2X thru cross at 44 GHz and does not comply with IEEE 370
- Via transition not optimized and has a remaining via stub

Outline

- The Intel Delta-L Methodology
  - Test methodology
  - Eigenvalue de-embedding
  - Curve-fitting insertion loss
  - Design and de-embedding essentials for achieving a high-quality outcome at high-frequencies
- Some essentials
  - Making accurate S-parameter measurements
  - Determining the reference plane for high-quality de-embedding
  - causality/passivity
- Mitigating design and layout artifacts in the curve-fitting for IL
- 67 GHz Delta-L

Delta-L References Planes

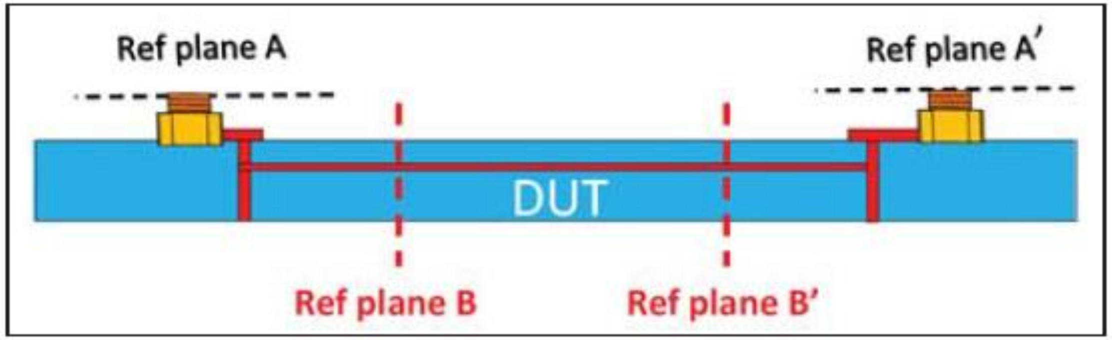


Figure 1-1 Reference Planes in Printed Board Insertion Loss Characterization

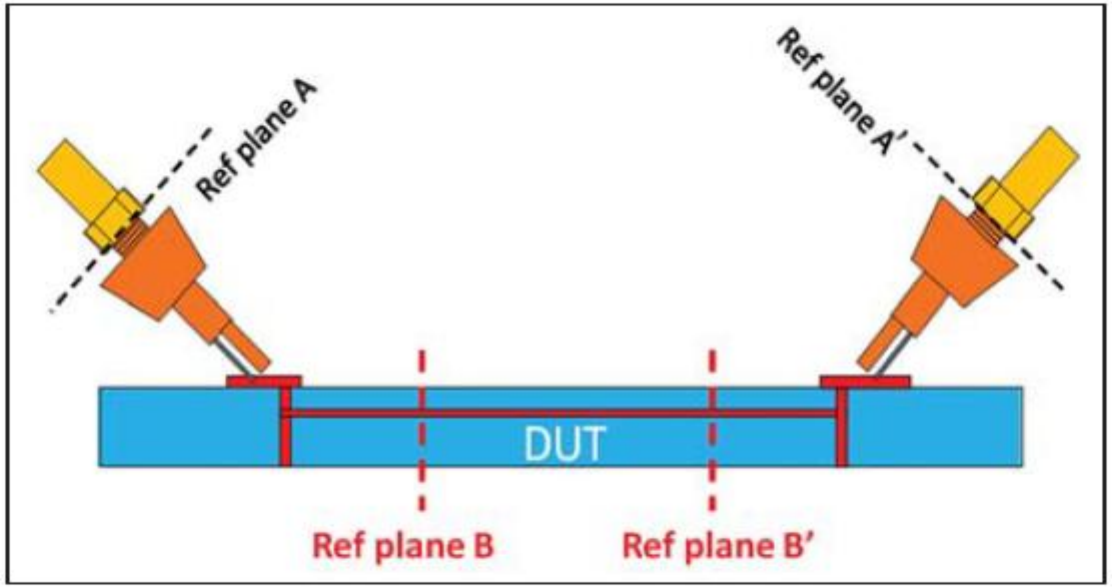


Figure 1-2 Reference Planes in Printed Board Insertion Loss Characterization with Microwave Probe

IPC-TM-650TEST METHODS MANUAL, 2.5.5.14

Reference planes in all cases are TEM because they are at transmission-line planes

Eigenvalue De-embedding Method

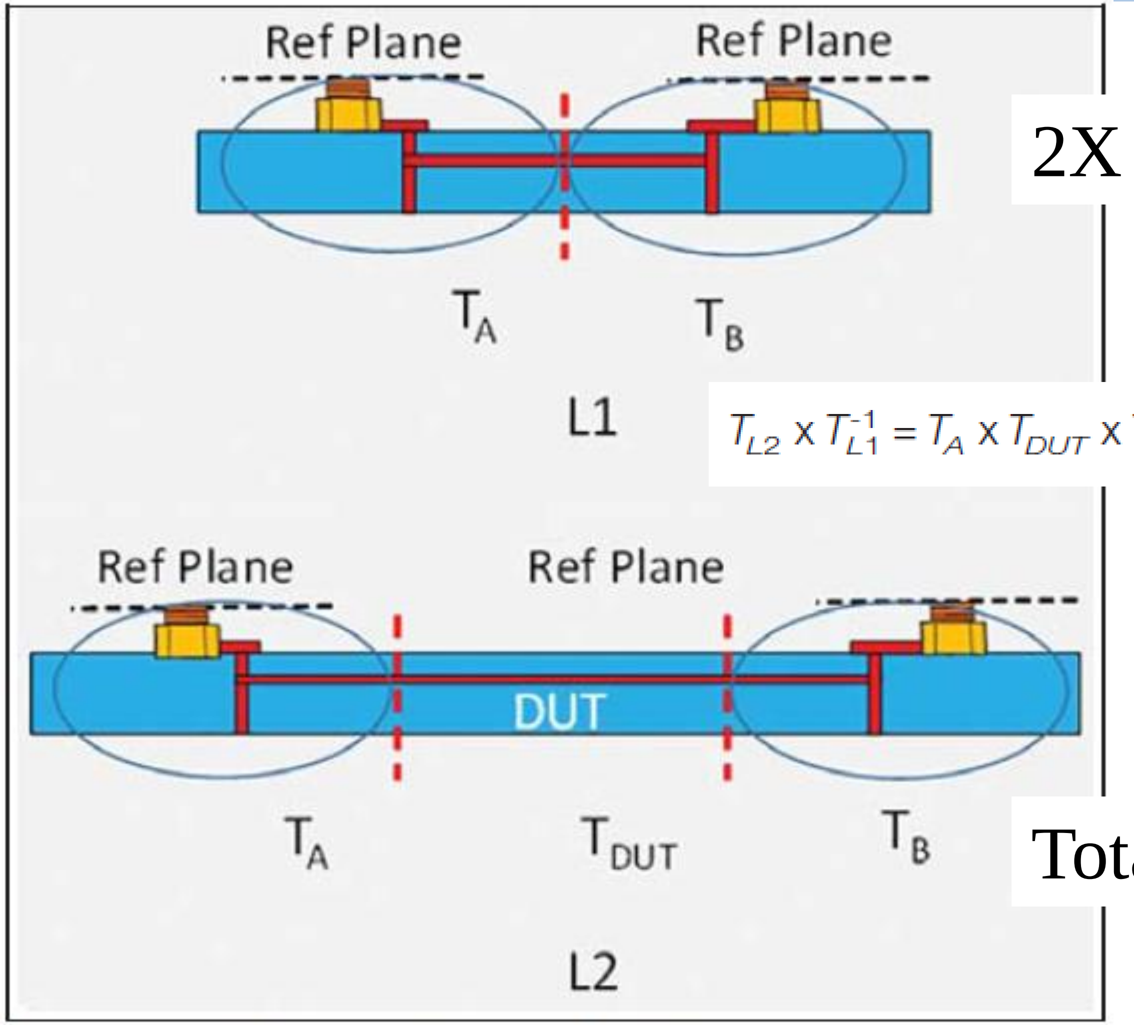


Figure 1-3 Two-line Structure for Eigenvalue-based Method

2X Thru

$$T_{L1} = T_A \times T_B \quad \text{(Eq. 2)}$$

$$T_{L2} = T_A \times T_{DUT} \times T_B \quad \text{(Eq. 3)}$$

$$T_{L2} \times T_{L1}^{-1} = T_A \times T_{DUT} \times T_B \times T_B^{-1} \times T_A^{-1} = T_A \times T_{DUT} \times T_A^{-1} \quad \text{(Eq. 4)}$$

$$T_{DUT} = \begin{bmatrix} e^{\gamma(L2-L1)} & 0 \\ 0 & e^{-\gamma(L2-L1)} \end{bmatrix} \quad \text{(Eq.5)}$$

Total structure

Calculation of Insertion Loss

$$T_{L1} = T_A \times T_B \quad \text{(Eq. 2)}$$

$$T_{L2} = T_A \times T_{DUT} \times T_B \quad \text{(Eq. 3)}$$

$$T_{L2} \times T_{L1}^{-1} = T_A \times T_{DUT} \times T_B \times T_B^{-1} \times T_A^{-1} = T_A \times T_{DUT} \times T_A^{-1} \quad \text{(Eq. 4)}$$

$$T_{DUT} = \begin{bmatrix} e^{\gamma(L2-L1)} & 0 \\ 0 & e^{-\gamma(L2-L1)} \end{bmatrix} \quad \text{(Eq.5)}$$

$T_{L2} \times T_{L1}^{-1}$ and T_{DUT} have the same eigenvalues.

Choose eigenvalue with absolute value <1 and real part is the attenuation.

Convert T-parameters to S-parameters:

$$S_{DUT} = \begin{bmatrix} 0 & e^{-\gamma L} \\ e^{-\gamma L} & 0 \end{bmatrix} \quad \text{(Eq.1)}$$

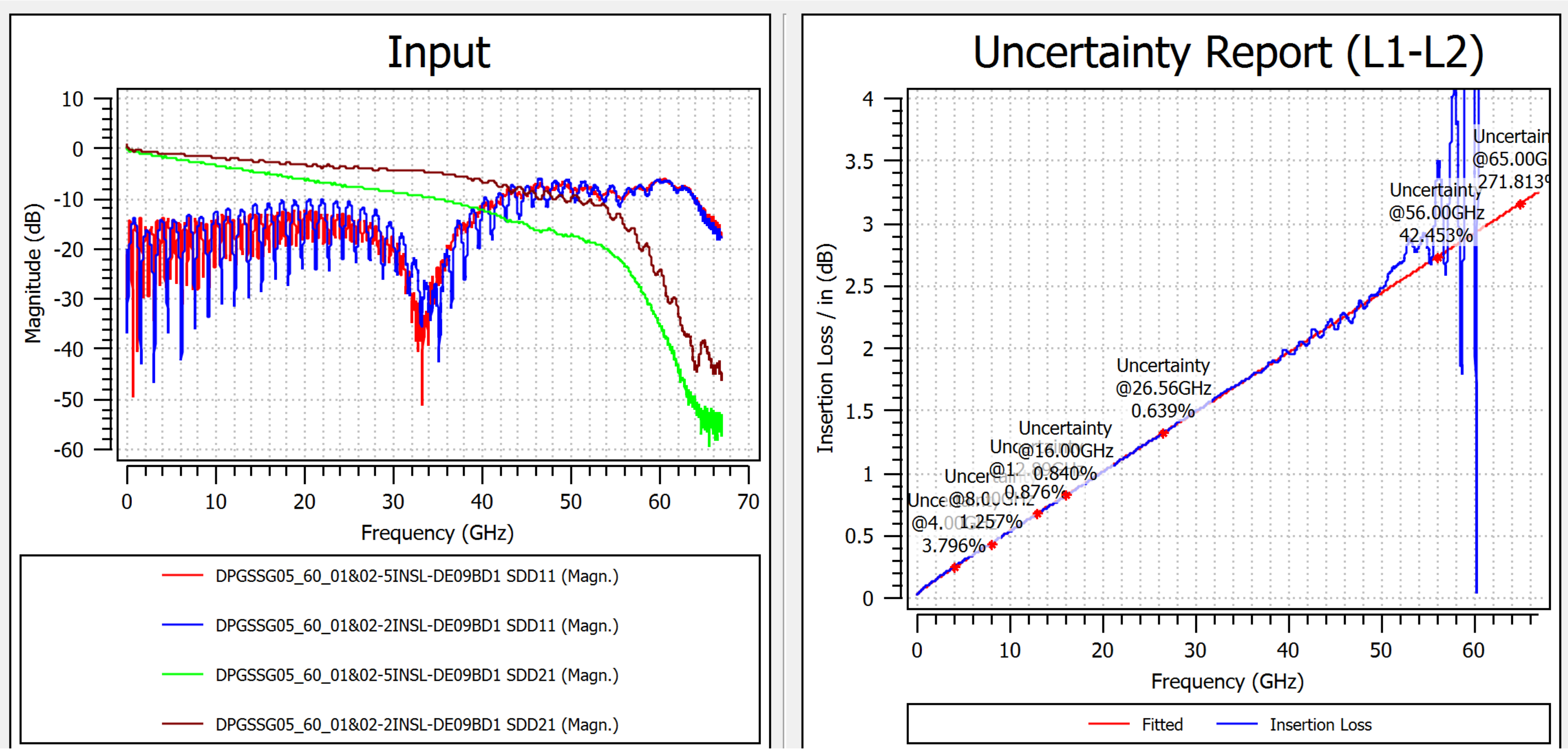
$$\gamma = \text{propagation constant} = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta$$

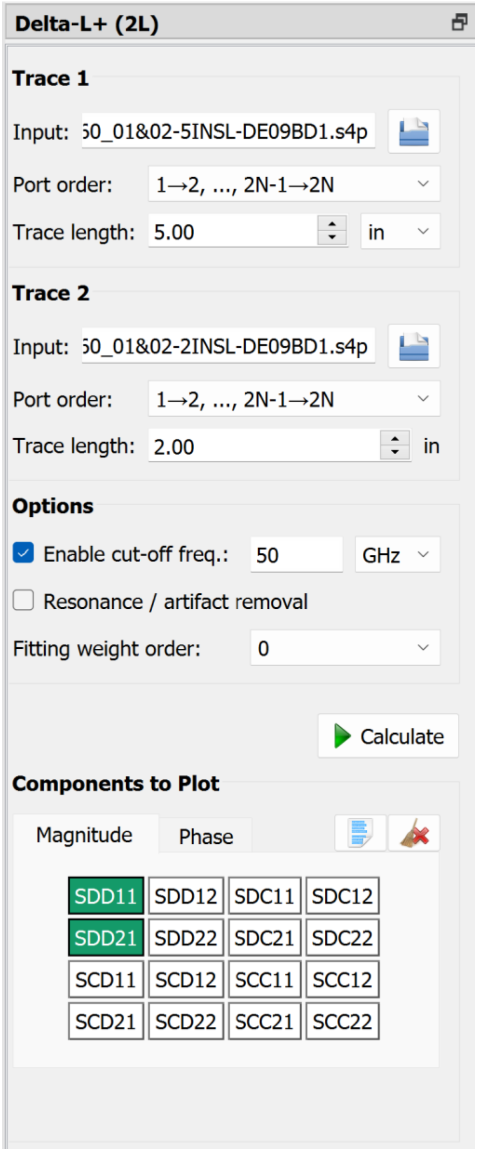
$\alpha \Rightarrow$ attenuation

$20\log_{10}(\alpha) \times length = IL$

IPC-TM-650TEST METHODS MANUAL, 2.5.5.14

Case 4 – Delta-L Outcome





— IL from eigenvalue de-embedding

— Fitted IL curve according to $IL_{dB}(f) = a(f - f_0)^b + c(f - f_0)^2 + d(f - f_0) + IL_0$

Note that above 50 GHz the de-embedding (blue curve) is becoming sensitive

Delta-L 4.0 Curve-Fitting

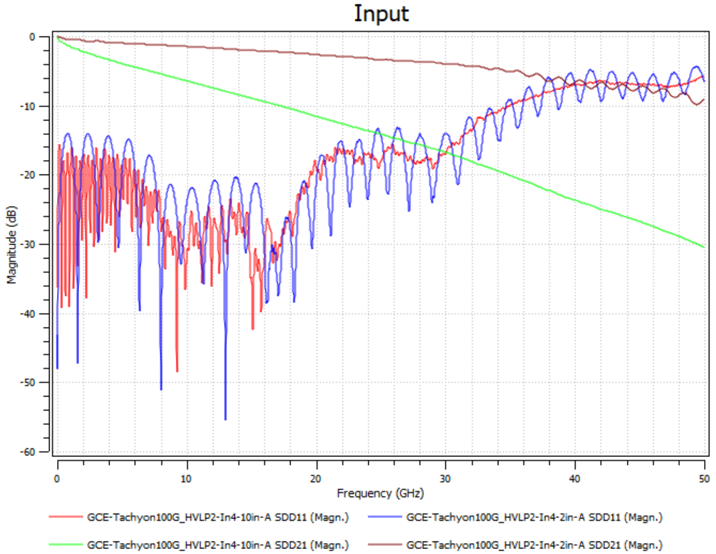
$$IL_{dB}(f) = \underbrace{a(f - f_0)^b}_{\text{Conductor loss}} + \underbrace{c(f - f_0)^2 + d(f - f_0)}_{\text{Dielectric loss}} + IL_0$$

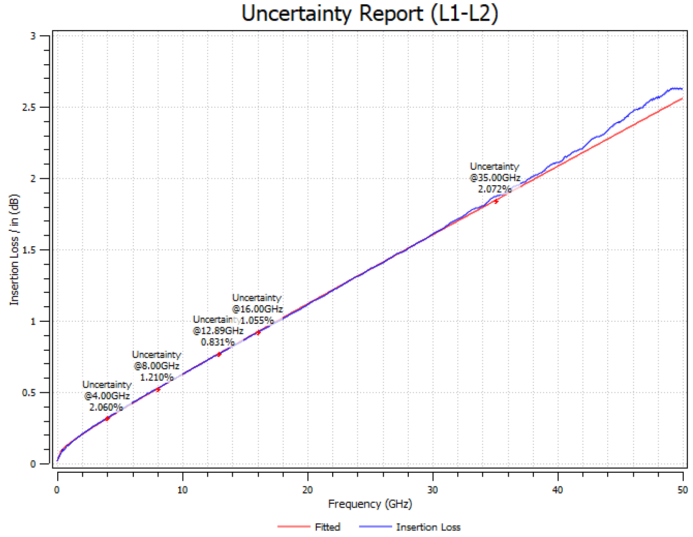
Conductor loss, including surface roughness

Dielectric loss

IPC-TM-650TEST METHODS MANUAL, 2.5.5.14

- f_0 and IL_0 are introduced as offsets to accommodate typical 10 MHz starting points for VNA measurements
- For a perfectly smooth conductor b=0.5





Weighting Factor for Curve-Fitting – IPC TM-650 2.5.5.14

$$W(f) = \left(1 - \left(\frac{f}{f_{max}}\right)\right)^3 \quad \text{(Eq.9)}$$

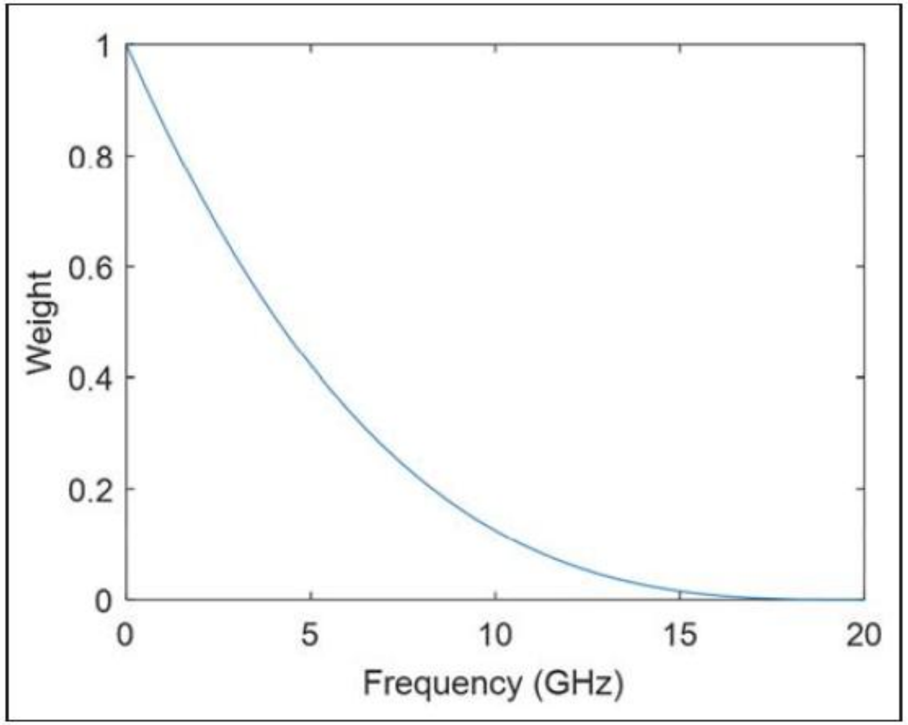


Figure 5-3 The Suggested Weight Function for Insertion Loss Curve Fitting

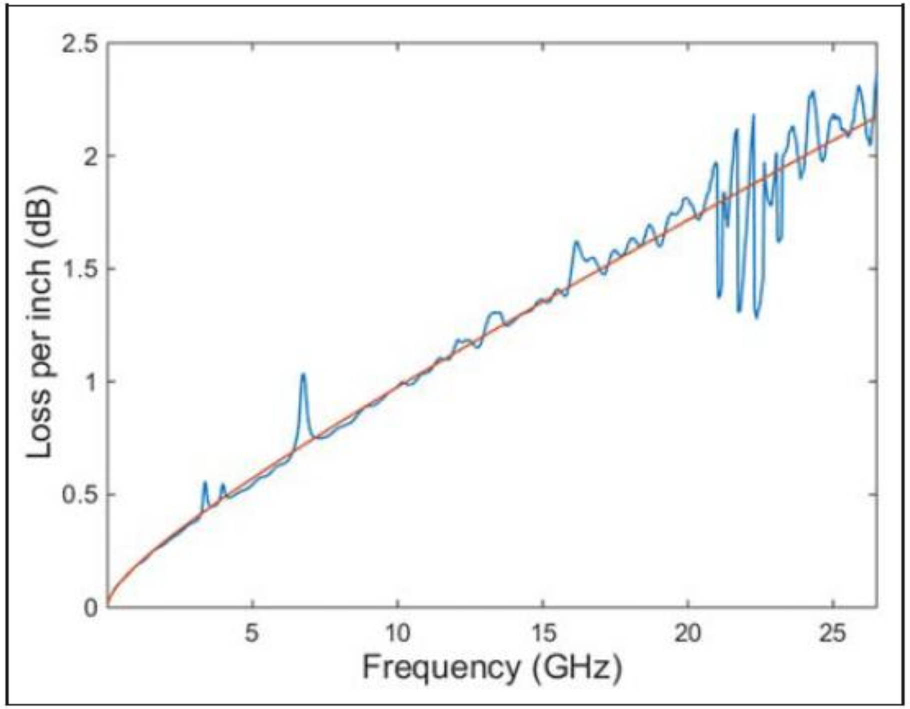


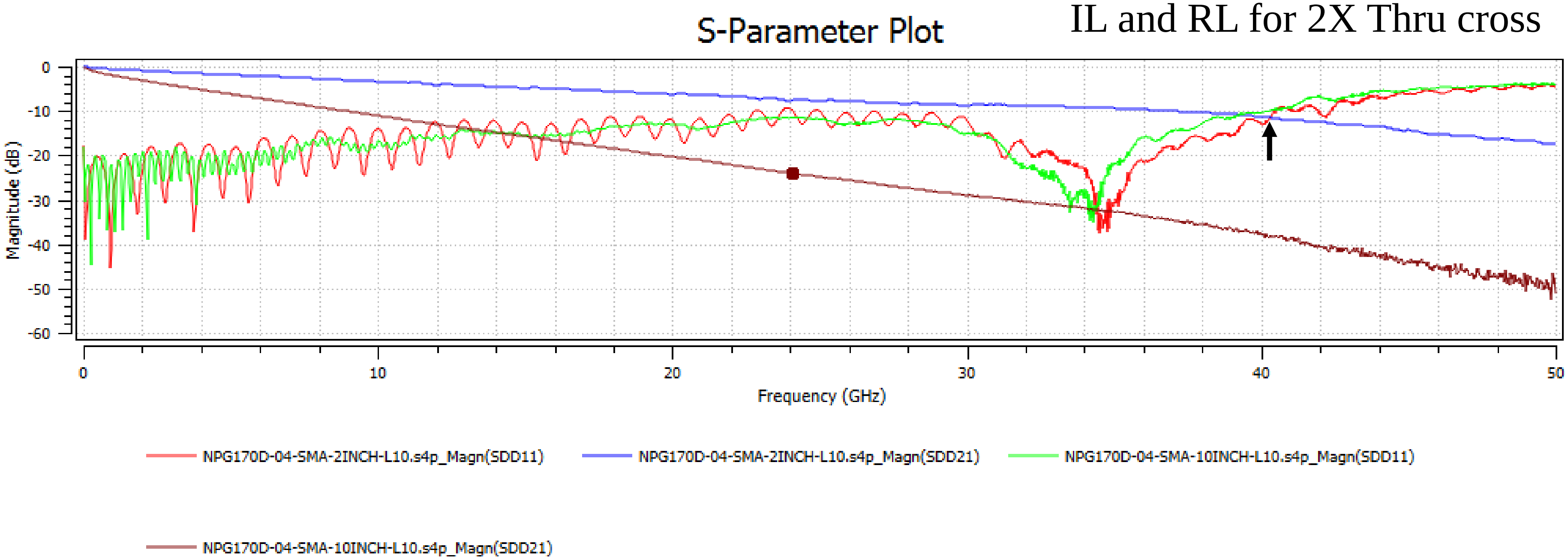
Figure 5-2 Least Squares Fit Based on (eq. 7) Applied to a Representative Insertion Loss Curve

Note 1. Red represents the fitted curve.

IPC-TM-650TEST METHODS MANUAL, 2.5.5.14

Case 4 – 2X Thru Meeting IEEE 370 STD to 40 GHz

IL and RL for 2X Thru cross

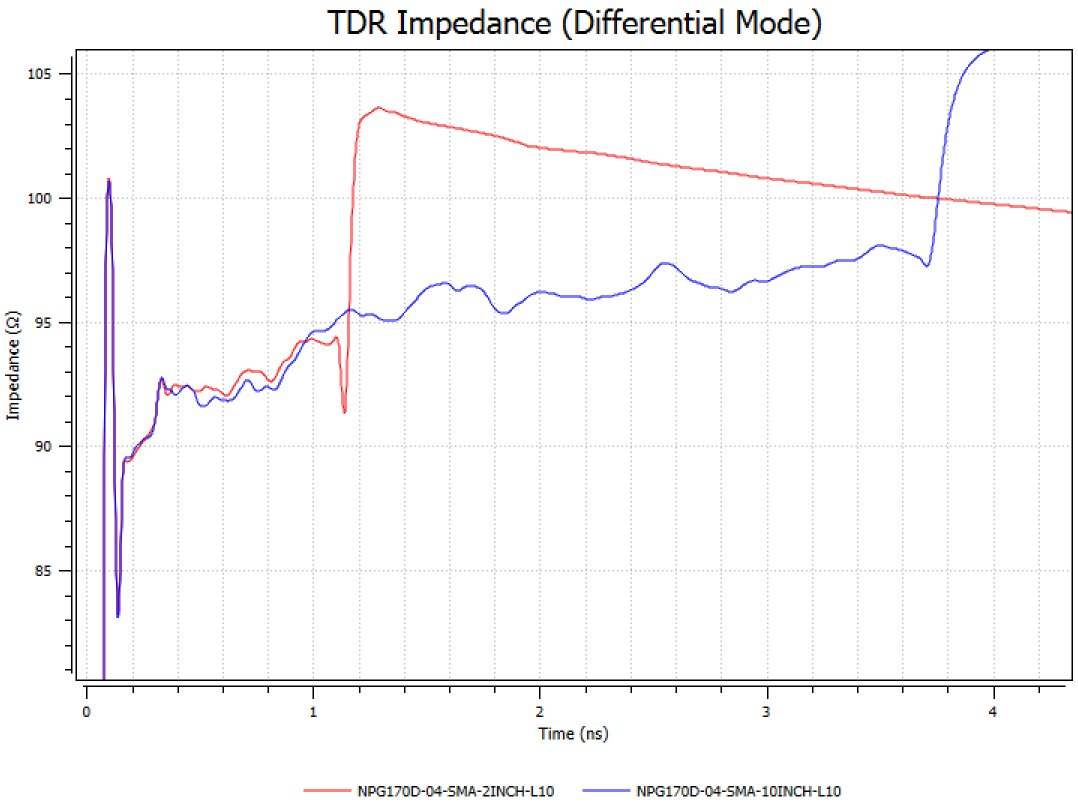


- The IL (blue) and RL (red) for the 2X Thru 2 in. stripline cross at 40 GHz
- The 2X Thru does not meet the IEEE 370 STD above and expect the de-embedding in Delta-L to become sensitive above 40 GHz with possibly resulting artifacts in the Delta-L 4.0 fit

Table 4—Fixture electrical requirement summary for mixed-mode interconnects

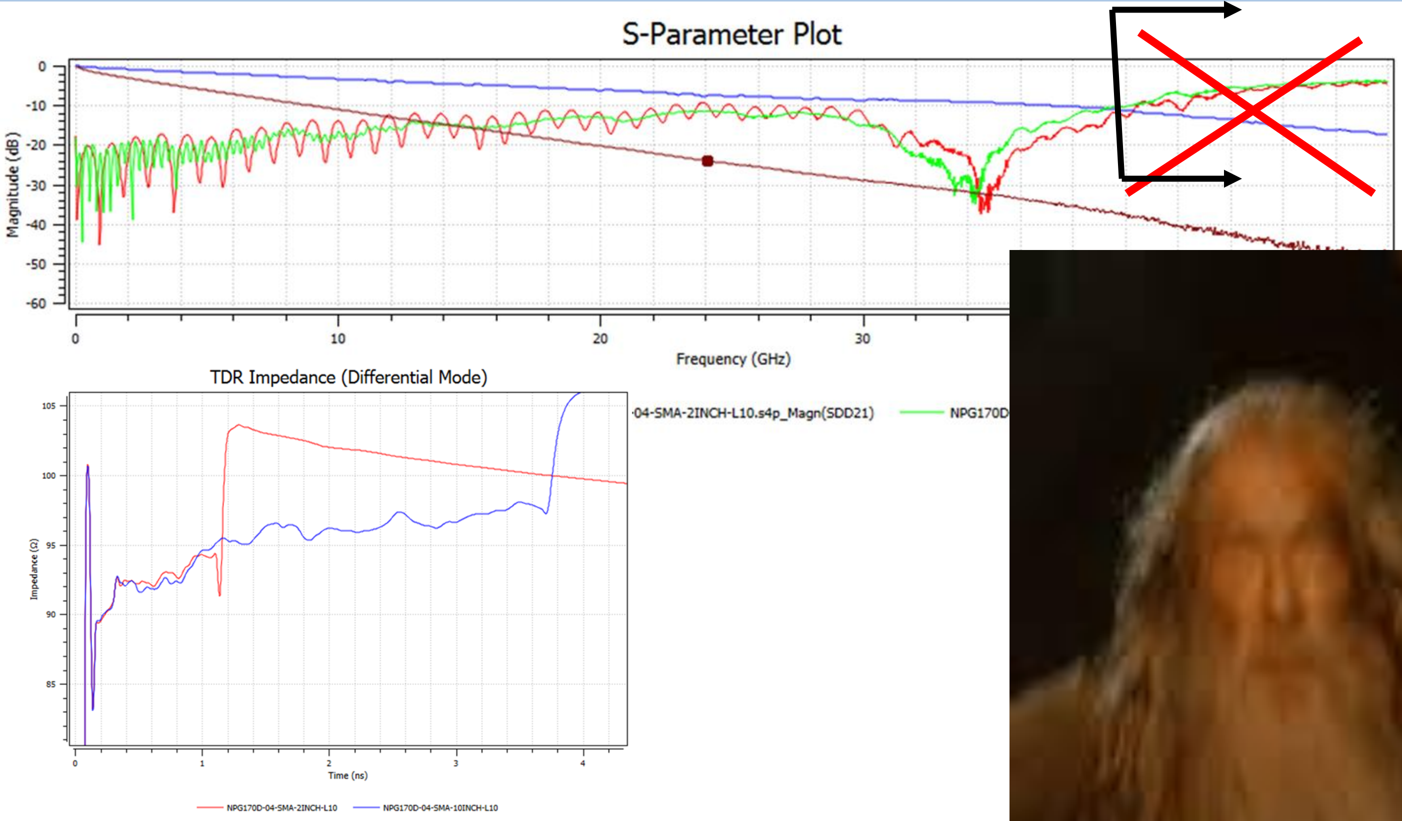
Metric	Structure	Equation	Class A limit	Class B limit	Class C limit
Insertion loss (FER1)	2X-Thru	$20\times\log_{10}\lvert S_{DD21}\rvert$	−10 dB	−15 dB	−15 dB
Return loss (FER2)	2X-Thru	$20\times\log_{10}\lvert S_{DD11}\rvert$	−20 dB	−10 dB	−6 dB
Difference between insertion and return loss (FER3)	2X-Thru	$20\times\log_{10}\lvert S_{DD21}\rvert - 20\times\log_{10}\lvert S_{DD11}\rvert$	5 dB	0 dB	0 dB

Case 4 – TDR



- The 2 in. and 10 in. traces are nearly identical in the transition and along the length. Will lead to better de-embedding and Delta-4.0 outcome.
- The transition from 100 Ω to 85 Ω is well engineered, but the stripline impedance target of 85 Ω was missed in manufacturing. If target were hit, Delta-L 4.0 outcome to 50 GHz would have been excellent.

De-Embedding is Sensitive when RL and IL of 2X Thru Cross



Crossing IL and RL of 2X Thru:

- 2X Thru is too long and IL is higher
- Transition from connector or probes not optimized resulting in higher RL at high frequencies.
- Missed line impedance of design in manufacturing

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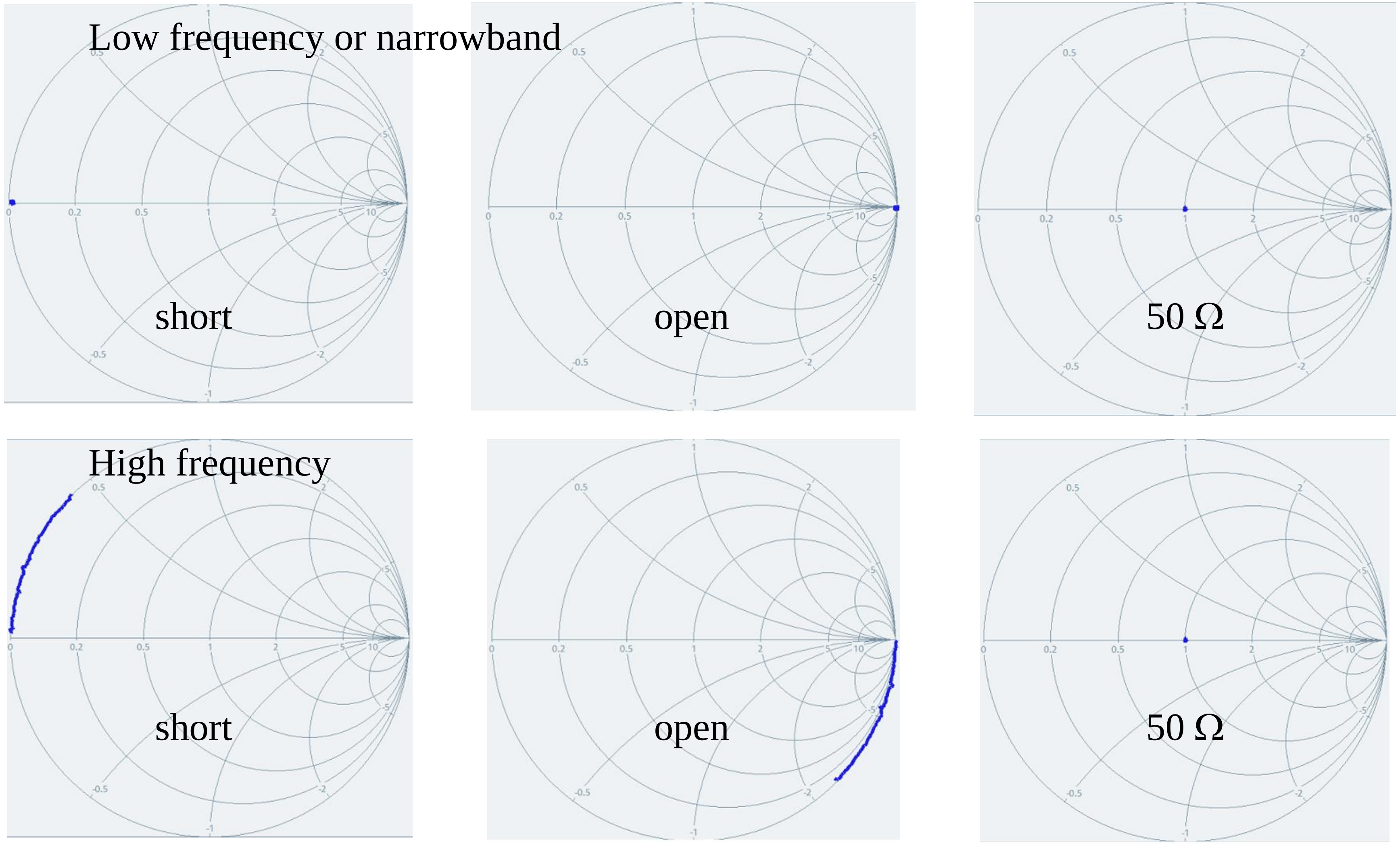
- 67 GHz Delta-L

Making Accurate S-parameter Measurements

- **Suitable high-frequency cables with precision connectors and precision adapters that are clean, maintained and not worn**
- **Have a mechanically stable measurement setup and avoid movement of cables and the DUT – plan the layout** (make good use of “painter’s tape to secure cables and test fixtures)
- Proper calibration coefficients for the cal kit
- Only the connector nut should be moving when mating a connector pair.
- Use proper torque wrenches
- Warm up the VNA per manufacturer’s specs before calibrating and measuring
- Calibrate the VNA immediately prior to measurements
- Use cal kits with care – they are relatively fragile, and regularly have them re-characterized per specs

Sanity Checks for Calibration

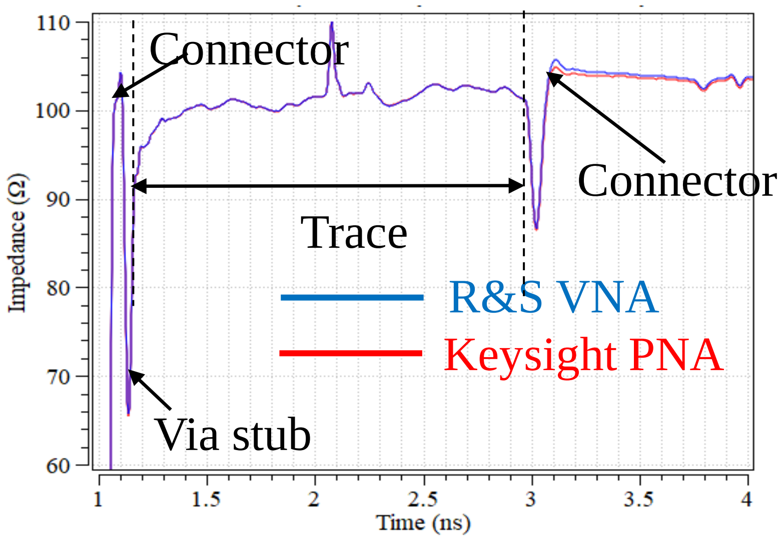
- Put the calibration standards back on and view on the Smith Chart to ensure that short, open, and load calibrations are "true"

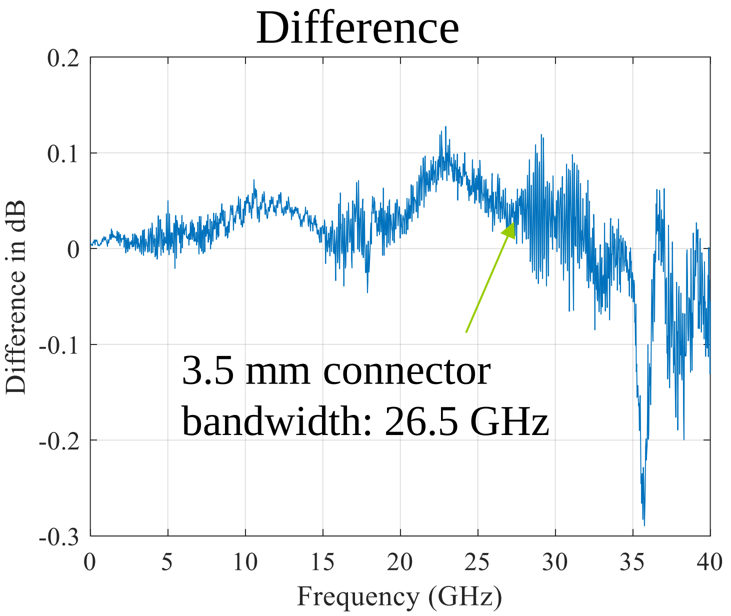


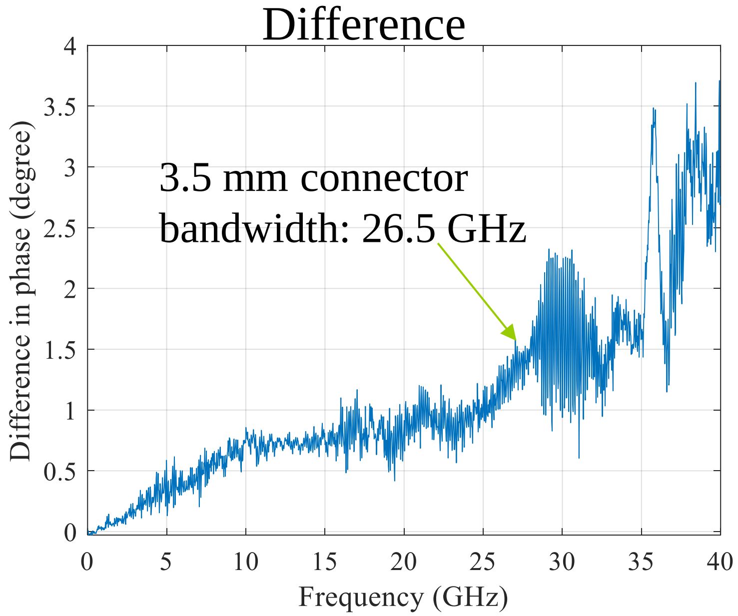
Comparison of Two Different Vendor VNAs

Rohde & Schwarz ZNB 40
(100KHz – 40GHz)

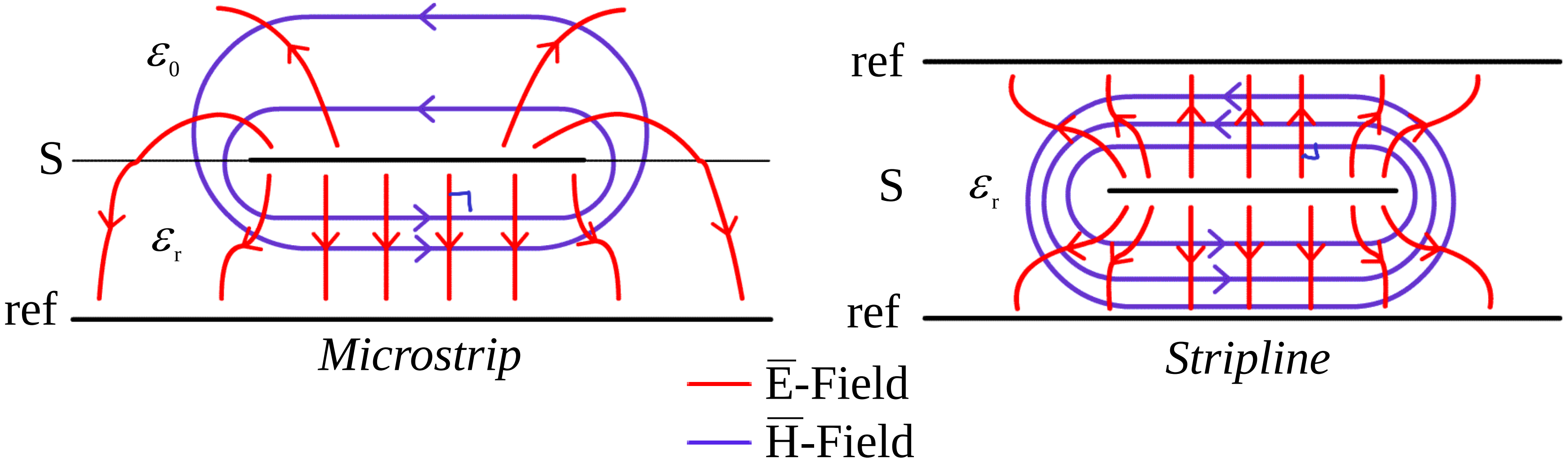
Two adaptors are used, a 2.4 M to 3.5 F, and a 3.5M to 3.5 M.





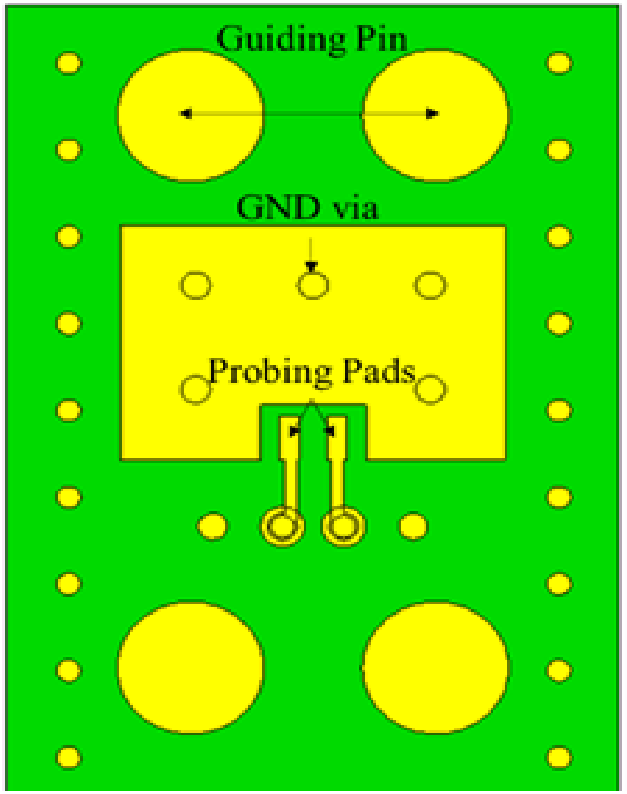


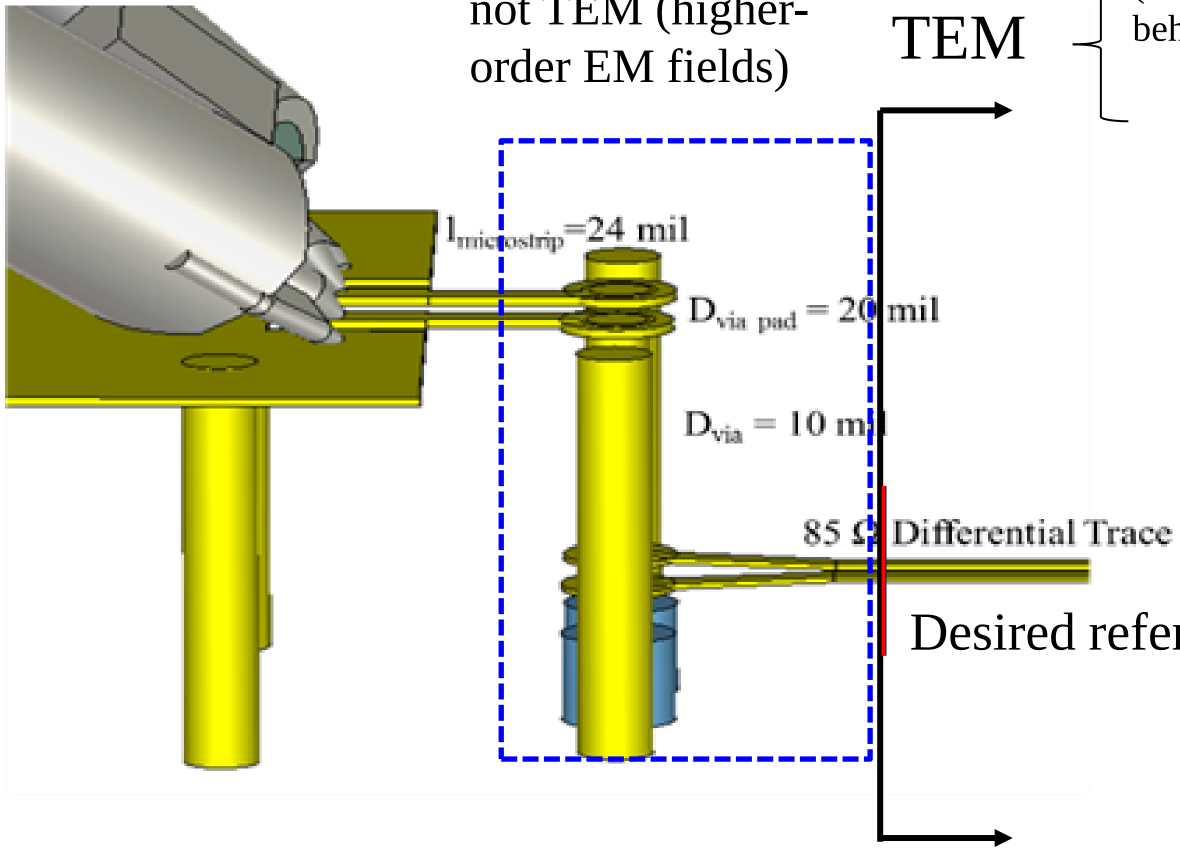
TEM – Transverse Electromagnetic Propagation



- **Transverse Electromagnetic (TEM) waves have the electric- and magnetic-field lines perpendicular, and E x H is in the direction of propagation.**
- **The geometry for a TEM transmission-line is translationally invariant, i.e., at every point along the length of the propagation, the cross-section geometry is the same**
- TEM waves have the property that the wave speed is the same for all frequencies (no dispersion for the ideal lossless case R = G = 0).
- Stripline supports a <u>pure</u> TEM wave (though PCB stripline is technically not pure TEM, but quasi-TEM), but microstrip is <u>quasi</u>-TEM.

TEM Boundary for Probing





not TEM (higher-order EM fields)

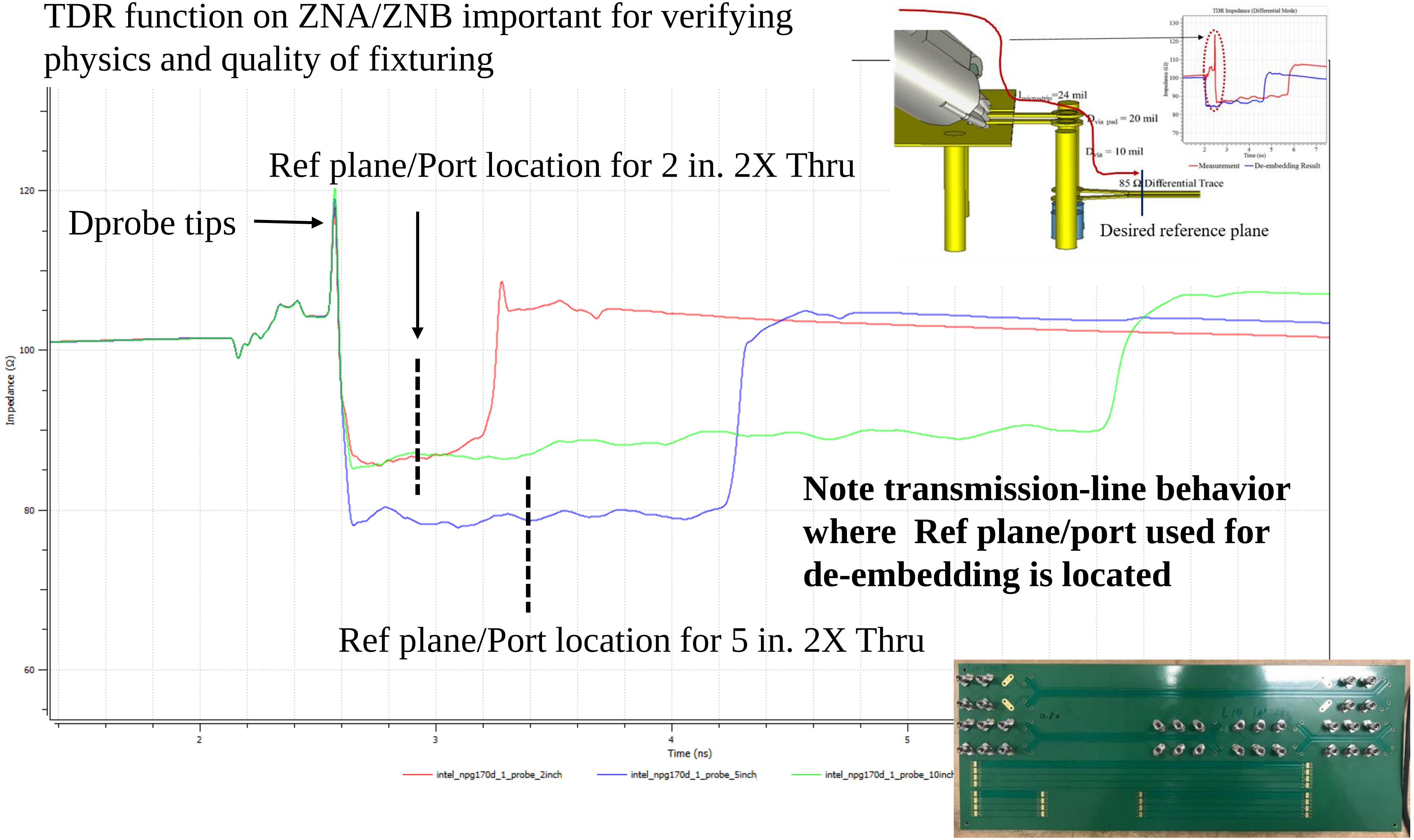
TEM

(Transmission-line behavior)

Desired reference plane

TDR for 2”, 5”, 10” for 85 Ω Differential Pair

TDR function on ZNA/ZNB important for verifying physics and quality of fixturing

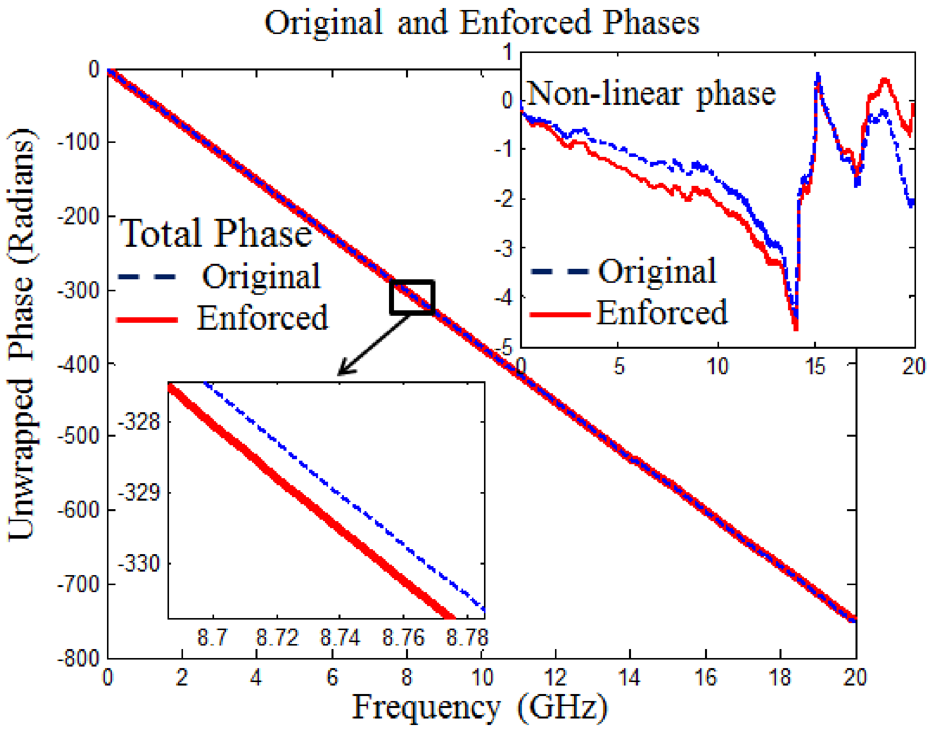


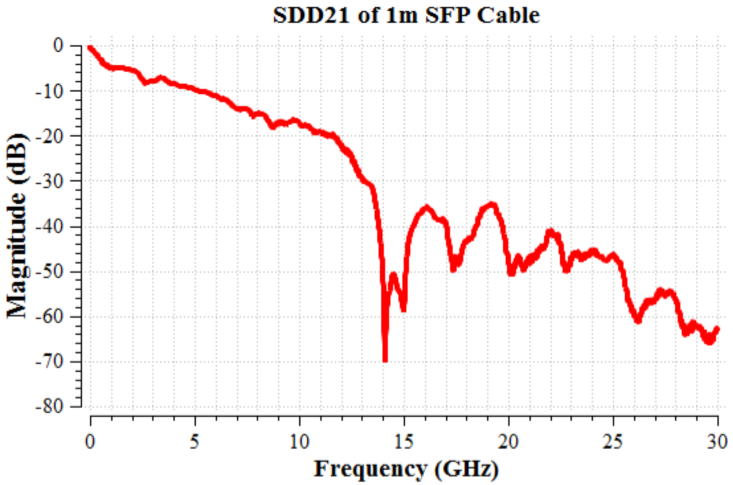
Note transmission-line behavior where Ref plane/port used for de-embedding is located

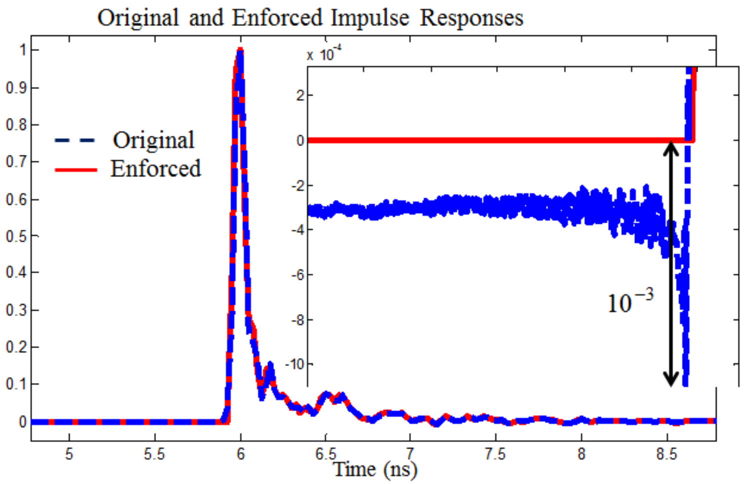
S-Parameters– Causality and Passivity Check – IEEE 370 STD

Causality and passivity should always be checked for S-parameters. (functionality provided in AITT)

- Measured 1m SFP cable
- Maintain magnitude and enforce phase for causality, or re-measure







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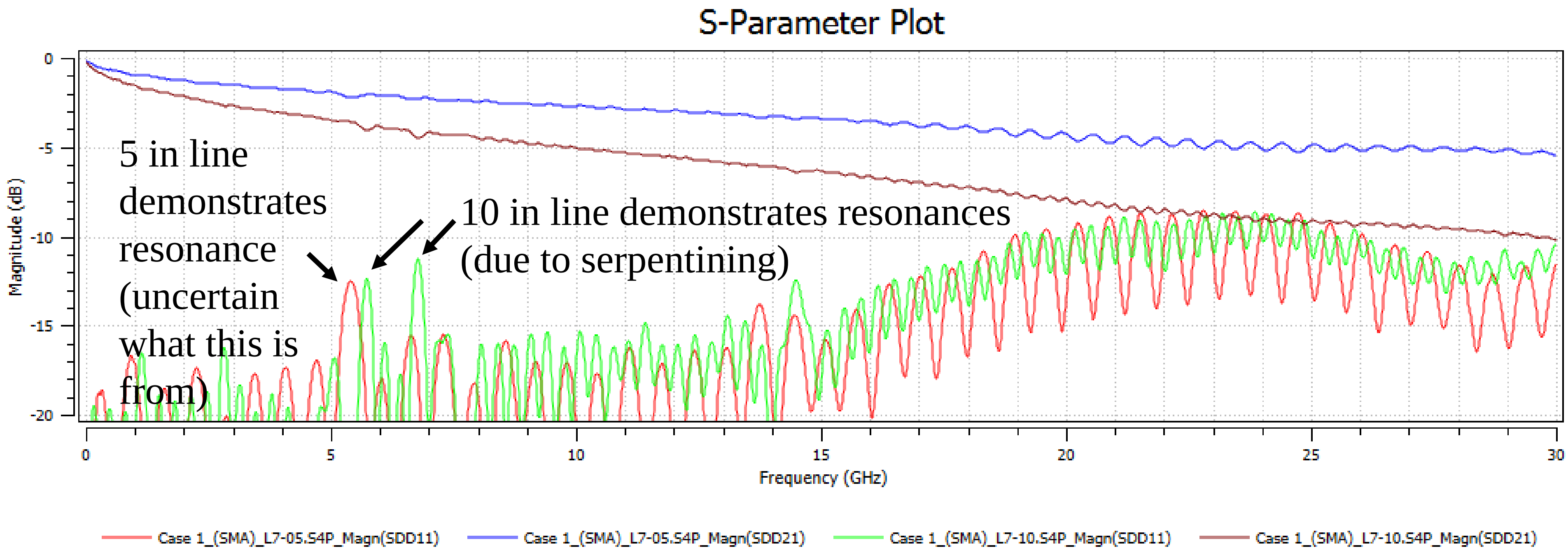
  - causality/passivity
- Mitigating design and layout artifacts in the curve-fitting for IL
- Moving toward 67 GHz Delta-L

Layout and Artifacts

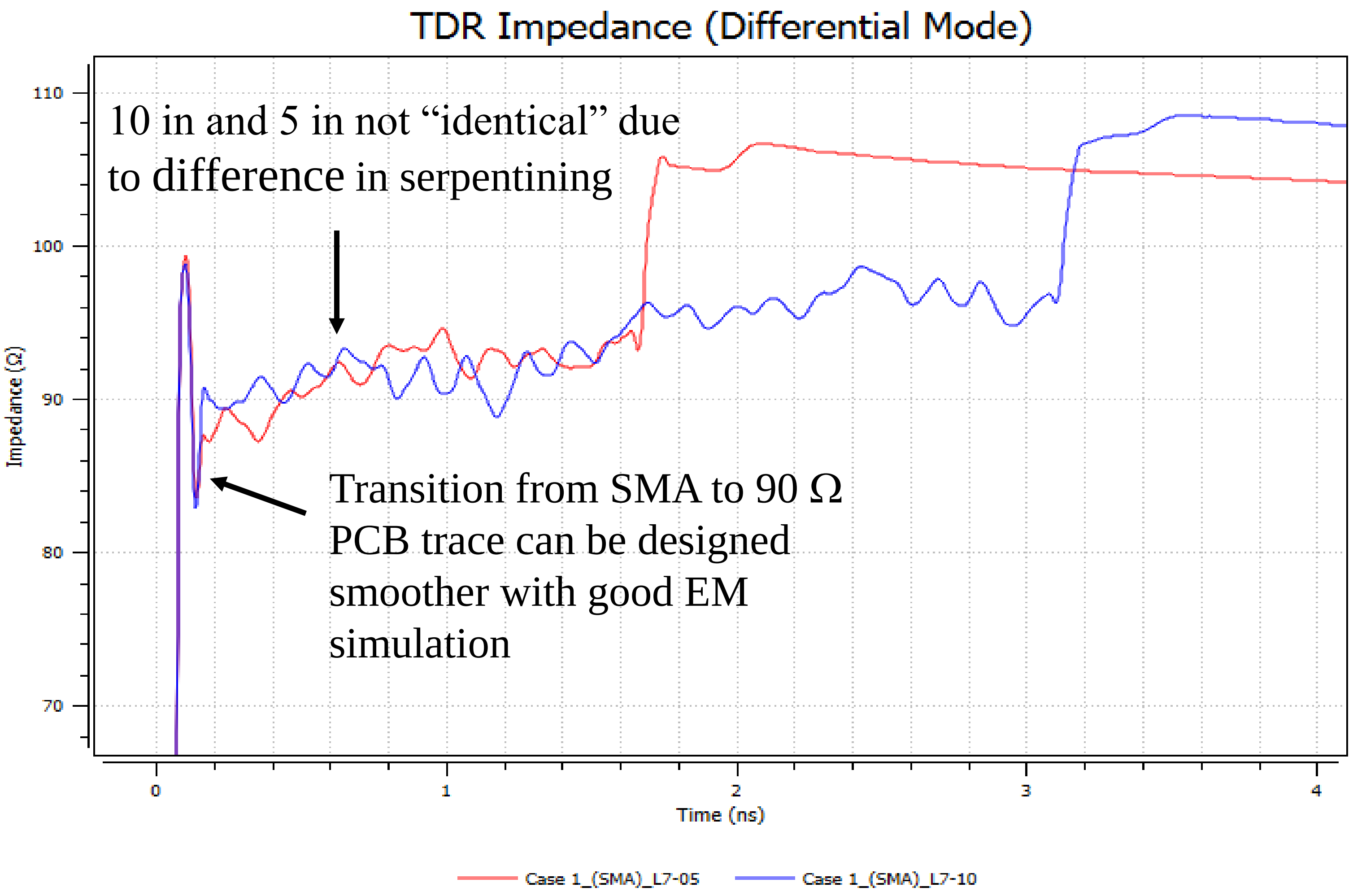
- Layout features can cause artifacts and resonances
  - Long serpentine traces leads to resonances
  - Insufficient ground vias at signal layer transitions can lead to a parallel-plate resonance that couples to the stripline being measured
- Best practices
  - Straight traces (at 67 GHz shorter traces will be necessary anyway and save space)
  - Universal footprint that ensures good signal return (GND) at the via transition – development underway at Intel/PacketMicro/Clear Signal Solutions
  - Adequate ground stitching at via transition (this is part of the universal probe launch)
  - No via stubs
  - Via stitching that is randomized around a nominal spacing

Case 1 – Resonances Due to Serpentining: S-Parameters



- S-parameter data shows that design of transition to PCB from an SMA is fairly good
- S-parameter data meets IEEE 370 STD for de-embedding
- Resonances in data will be reflected in de-embedding and must be dealt with in loss fitting

Case 1 – Differential TDR

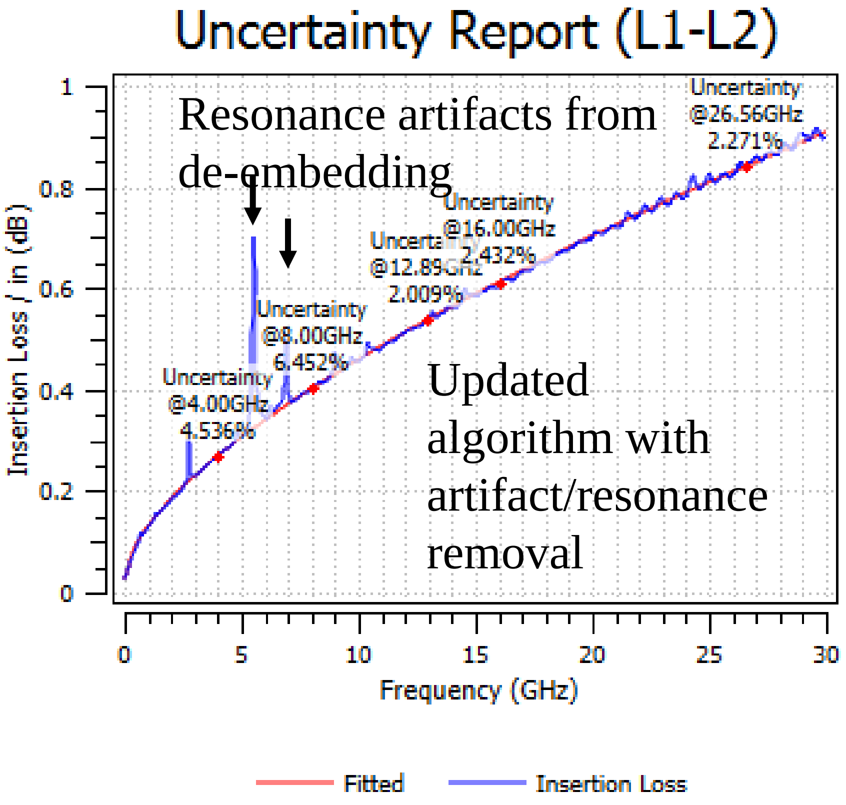


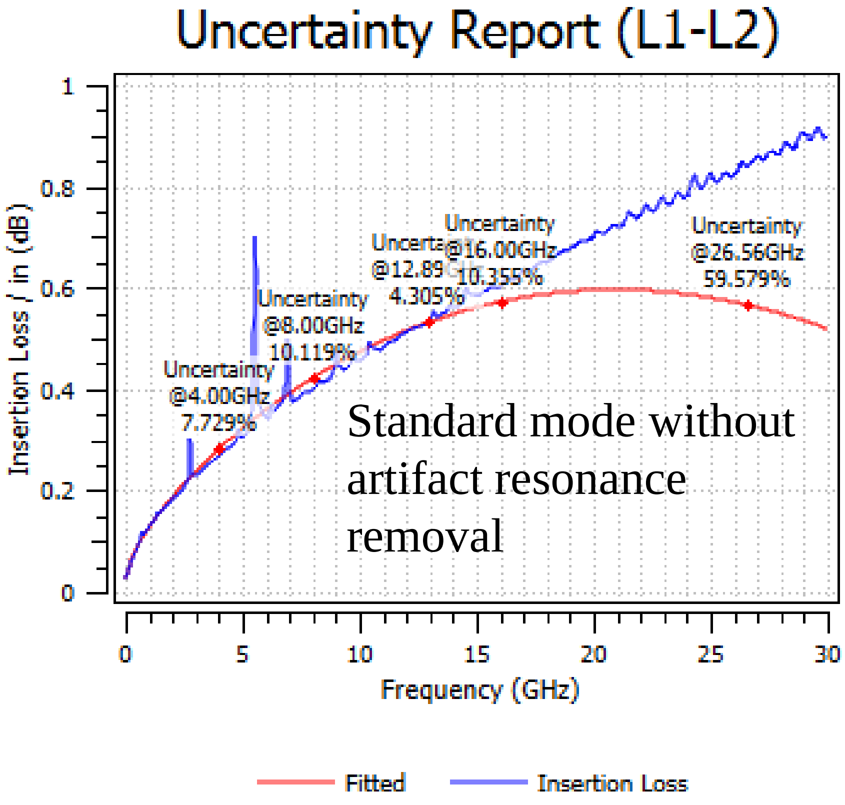
10 in and 5 in not “identical” due to difference in serpentining

Transition from SMA to 90 Ω PCB trace can be designed smoother with good EM simulation

Case 1 – Delta-L 4.0 with & w/o Resonance/Artifact Removal

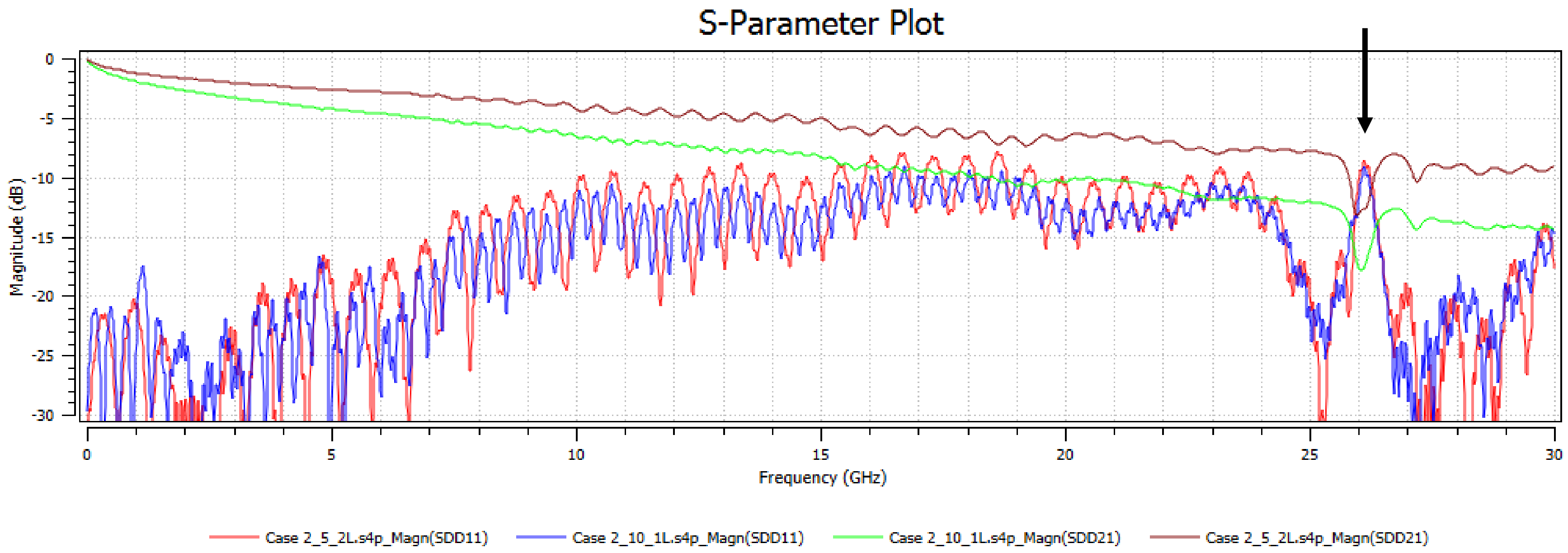
Have developed in AITT a curve-fitting routine that eliminates resonance and artifact skewing in the curve fitting





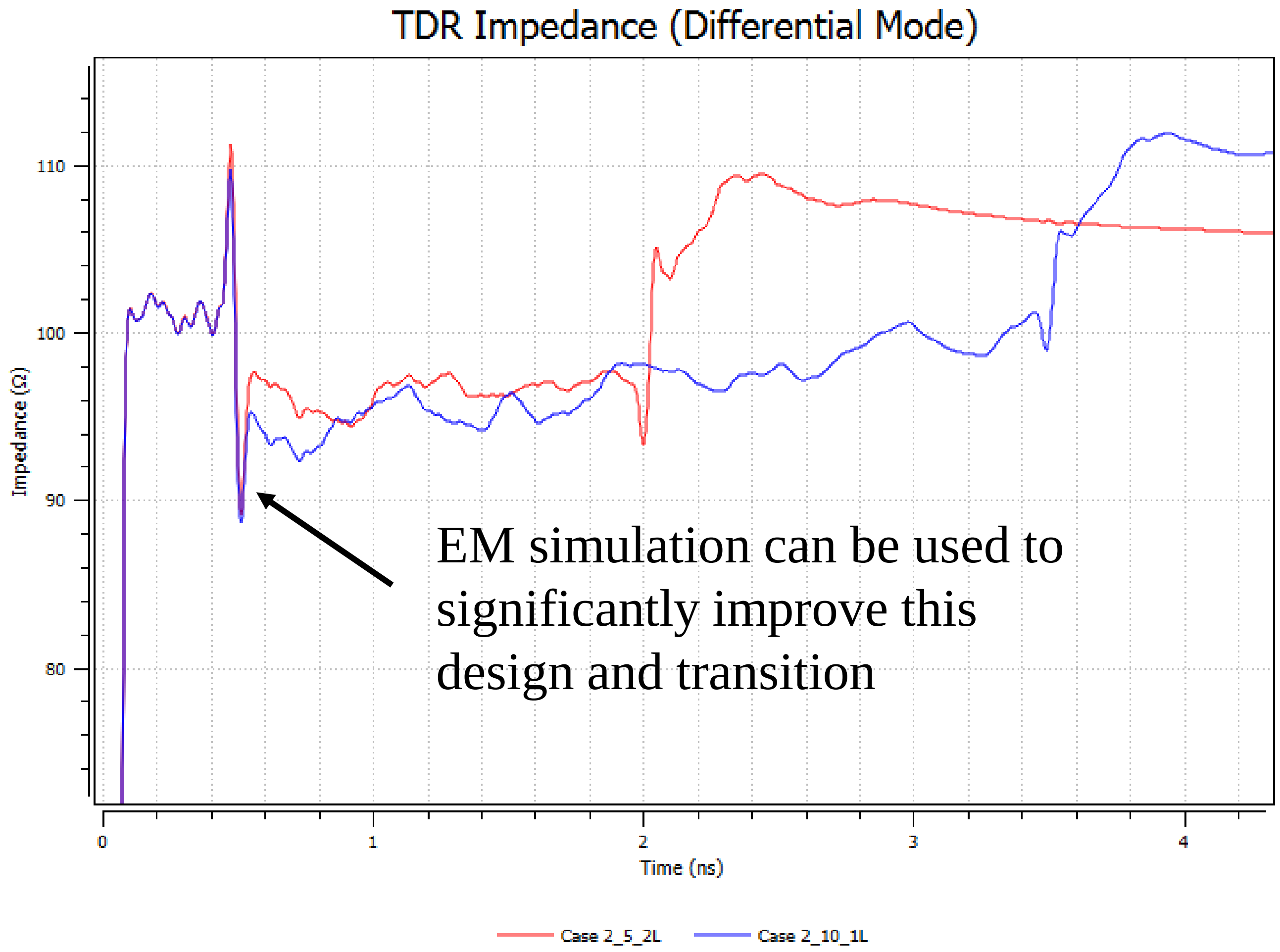
Case 2 – Coupling to Planes from Via Transition at Feed: S-Parameters

Resonance due to via transition at feed coupling to parallel-plate modes



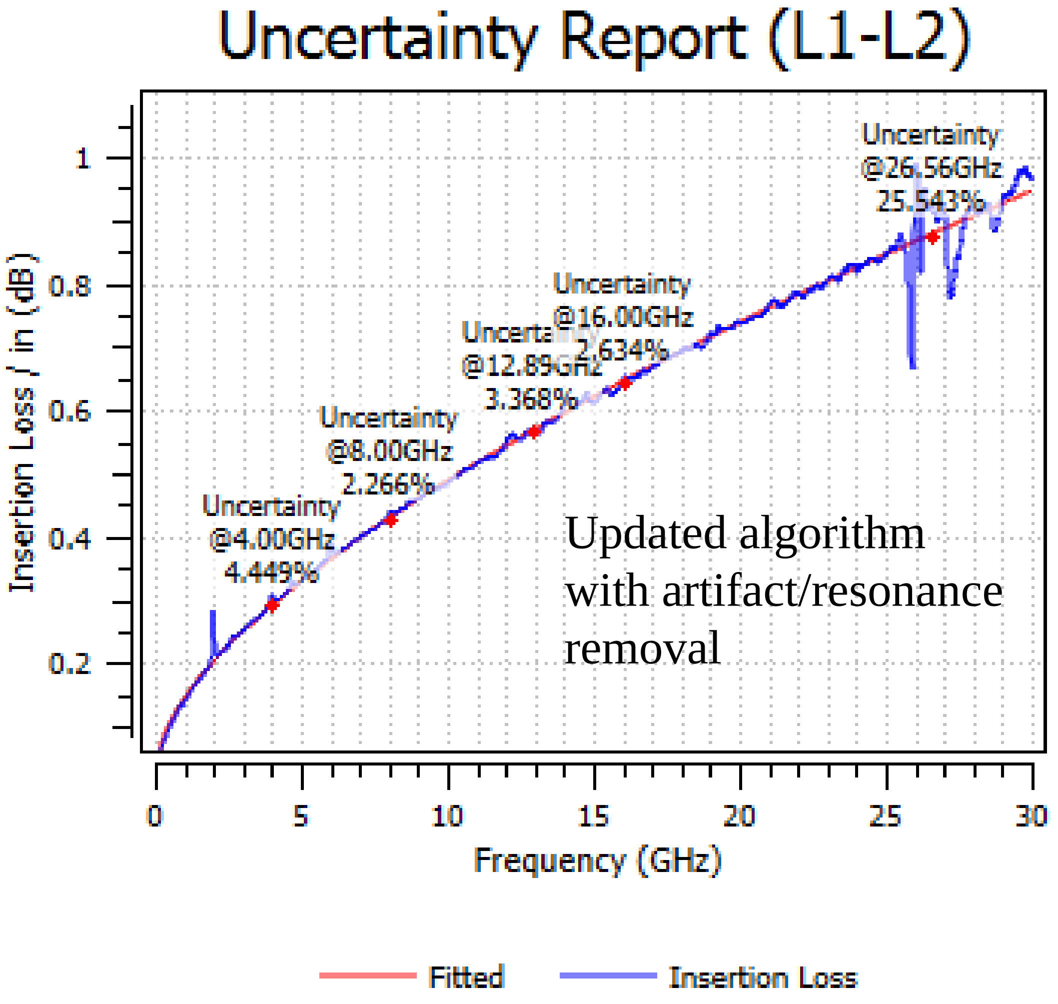
- Resonance due to via transition coupling to parallel plate modes will result in de-embedding sensitivity
- Crossing of IL and RL in the shorter 2X Thru (brown, red curves) will result in de-embedding sensitivity
- EM simulation can be used here to identify this resonance, its cause, and solution

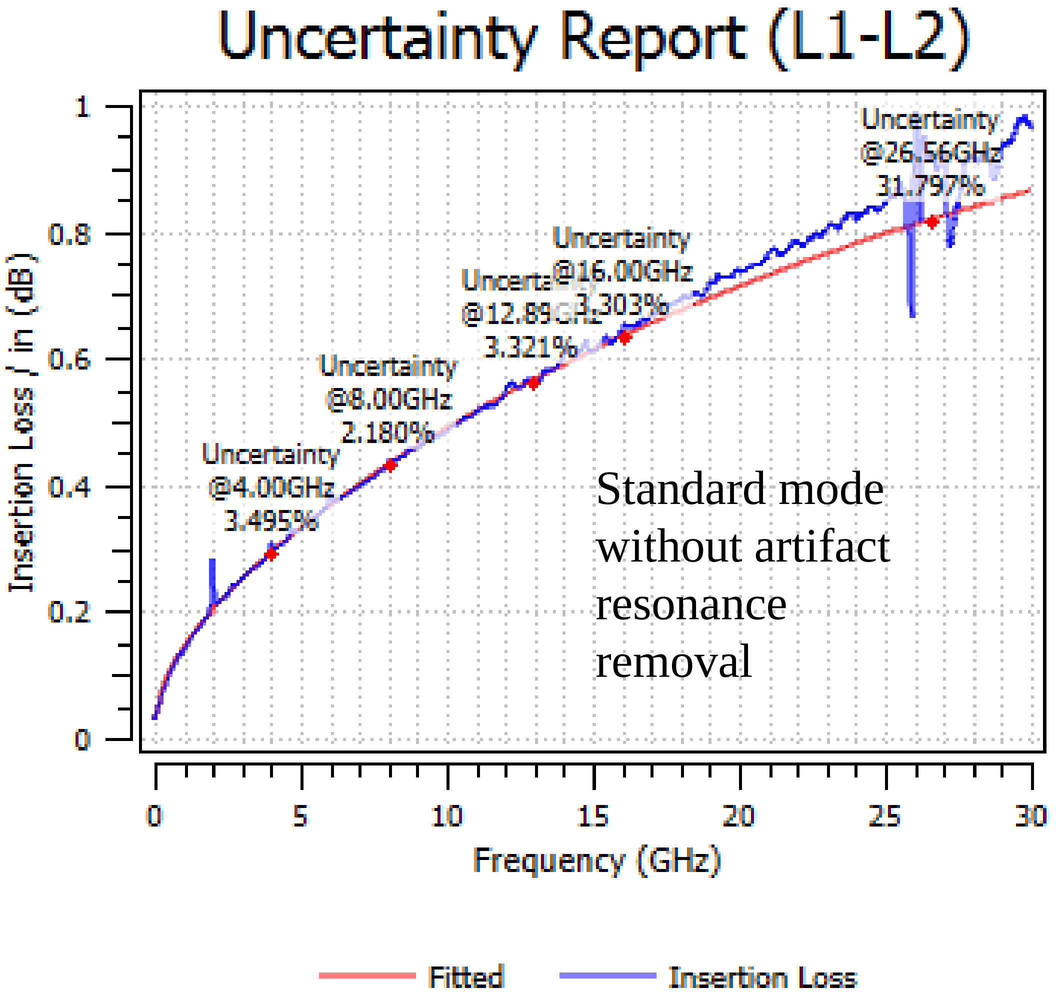
Case 2 - TDR



Parallel plate mode coupling to the signal trace is not readily apparent in the TDR

Case 2 - Delta-L 4.0 with & w/o Resonance/Artifact Removal





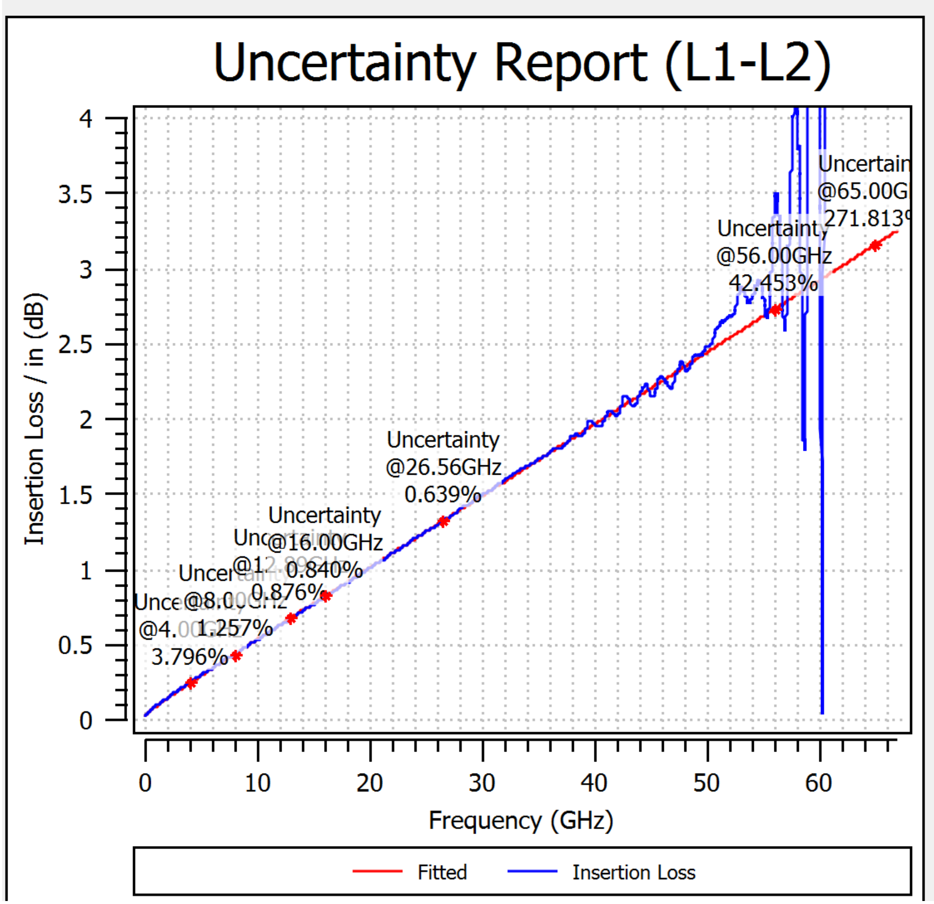
Modifying the Curve-Fitting Algorithm

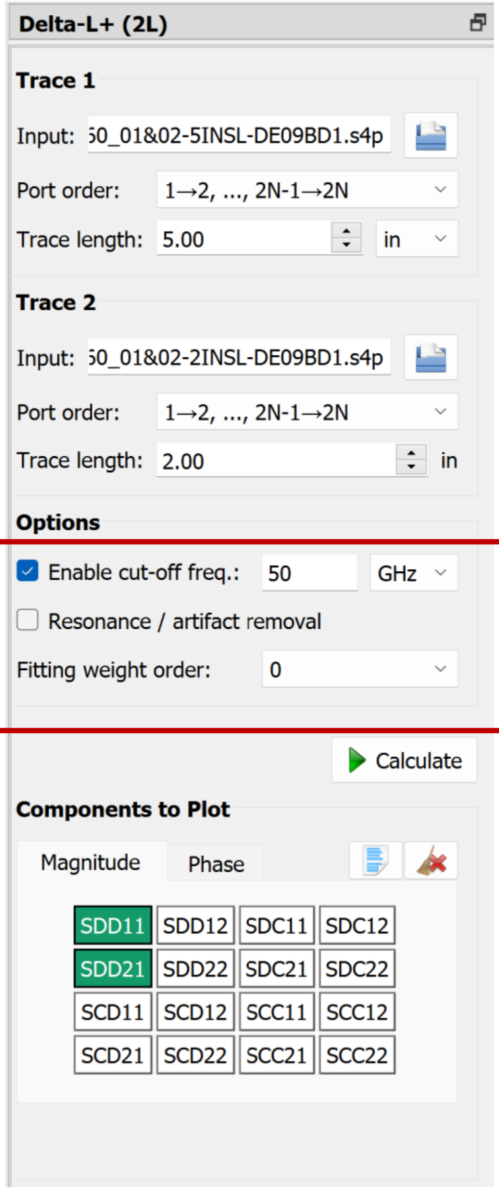
$$W(f) = \left(1 - \left(\frac{f}{f_{max}}\right)\right)^3 \quad \text{(Eq.9)}$$

IPC-TM-650TEST METHODS MANUAL, 2.5.5.14

$$W(f) = \left(1 - \left(\frac{f}{f_{max}}\right)\right)^n$$

Allow n = 0, 1, 2, or 3





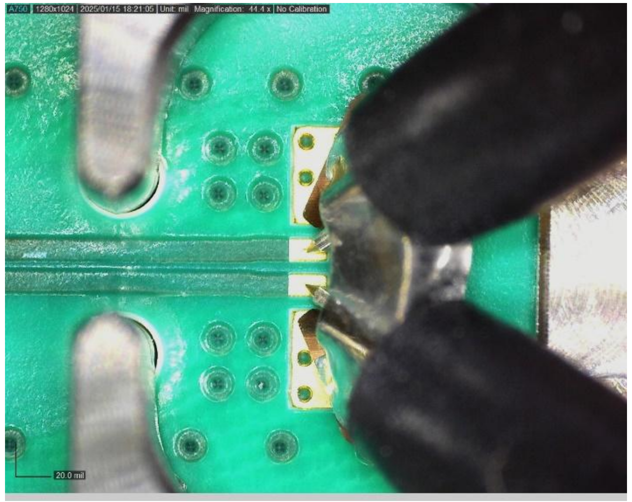
Outline

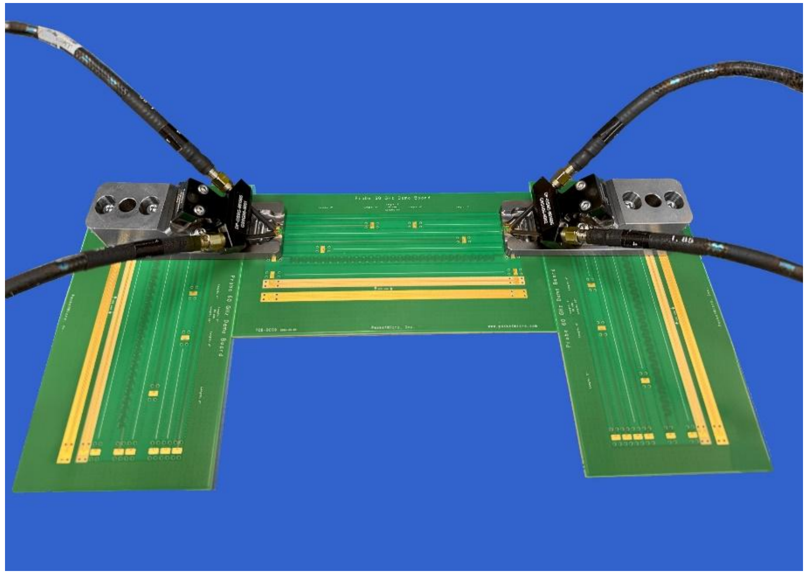
- The Intel Delta-L Methodology
  - Test methodology
  - Eigenvalue de-embedding
  - Curve-fitting insertion loss
  - Design and de-embedding essentials for achieving a high-quality outcome at high-frequencies
- Some essentials
  - Making accurate S-parameter measurements
  - Determining the reference plane for high-quality de-embedding
  - causality/passivity
- Mitigating design and layout artifacts in the curve-fitting for IL
- 67 GHz Delta-L

Summary for Achieving Delta-L to 67 GHz

- 0.5 mm probe pitch, hand-held probes with bases for use in large-volume measurements and in fabrication environment
- Optimized universal footprint to accommodate handheld probes and rapid alignment/placement
- Stripline lengths – meet IEEE 370 STD for de-embedding accuracy, e.g., 2” & 5”

PacketMicro 0.5 mm GSSG probes



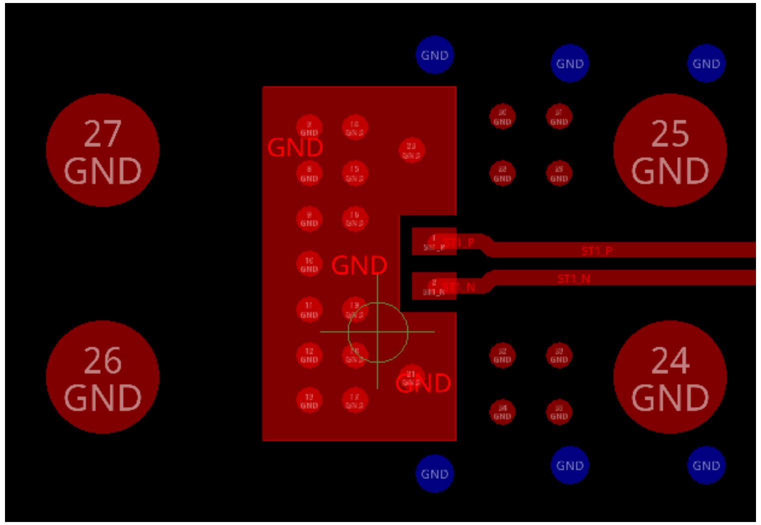


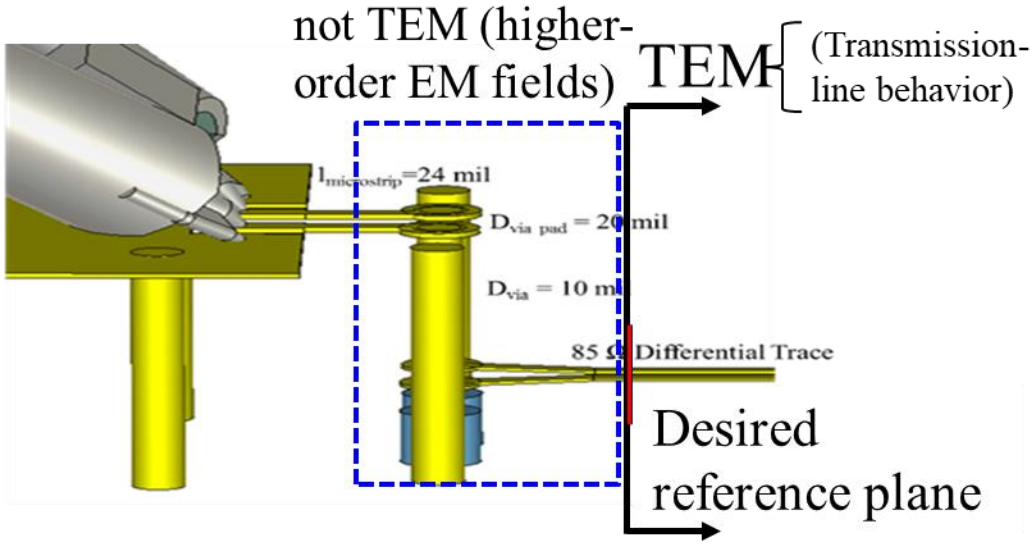
With bases for handheld placement with alignment holes

Establishing Best Practices

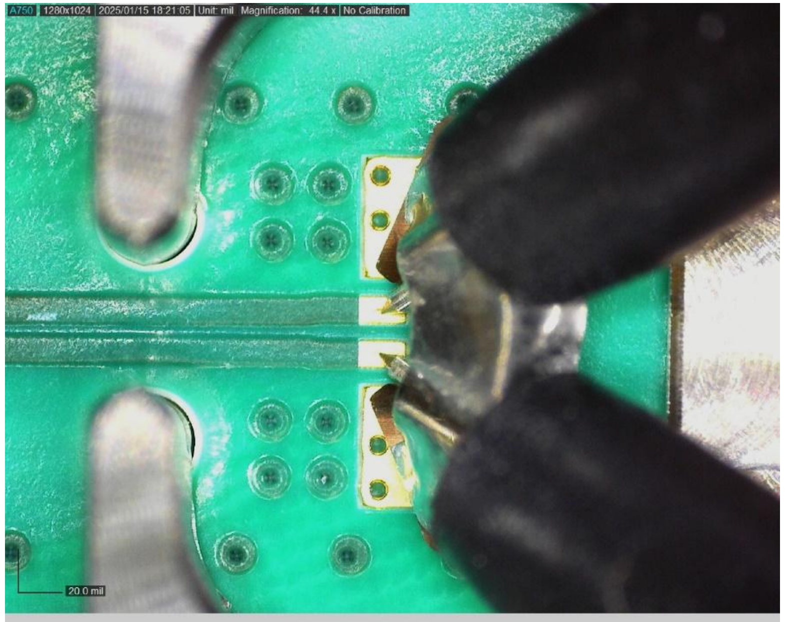
- Straight traces (at 67 GHz shorter traces will be necessary anyway and save space) to avoid resonances from serpentine layout
- Universal footprint that ensures good signal return (GND) at the via transition, i.e., well-designed ground return via pattern to avoid coupling to parallel-plate modes
- No via stubs
- Via stitching that is randomized around a nominal spacing
- Careful design with full-wave EM simulation to ensure all of the above

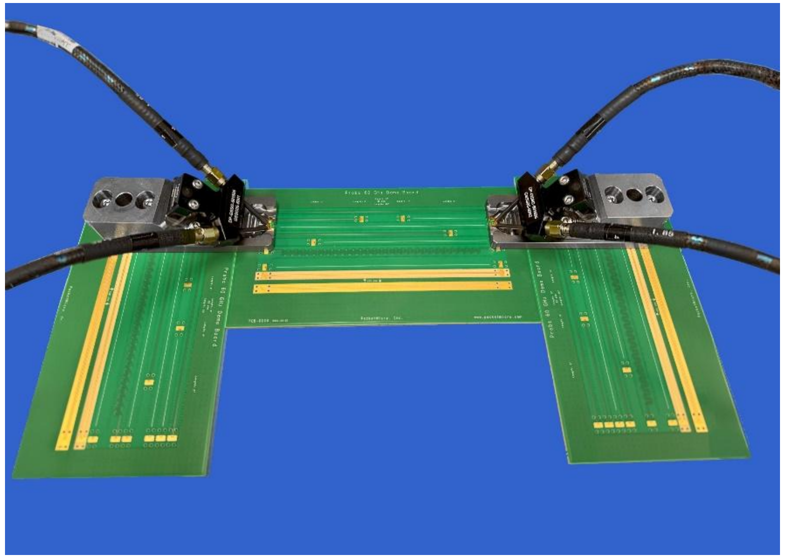
Intel Delta-L 4.0
(0.5 mm pitch)



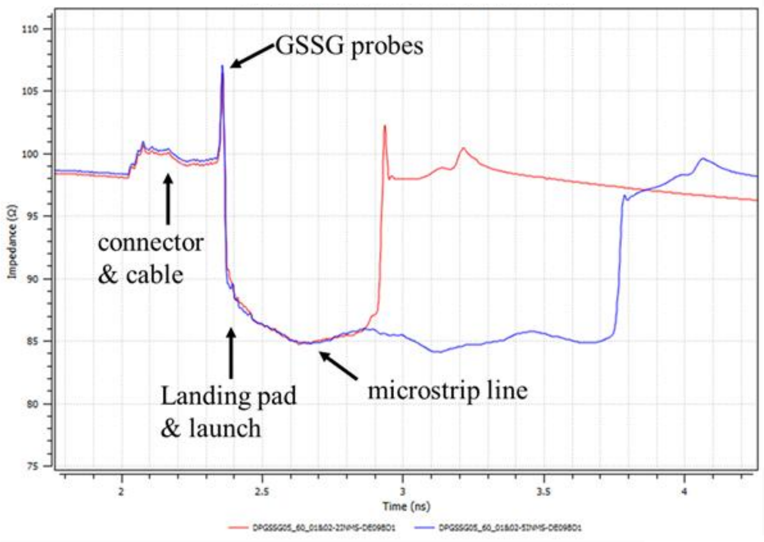


67 GHz PacketMicro GSSG Probe



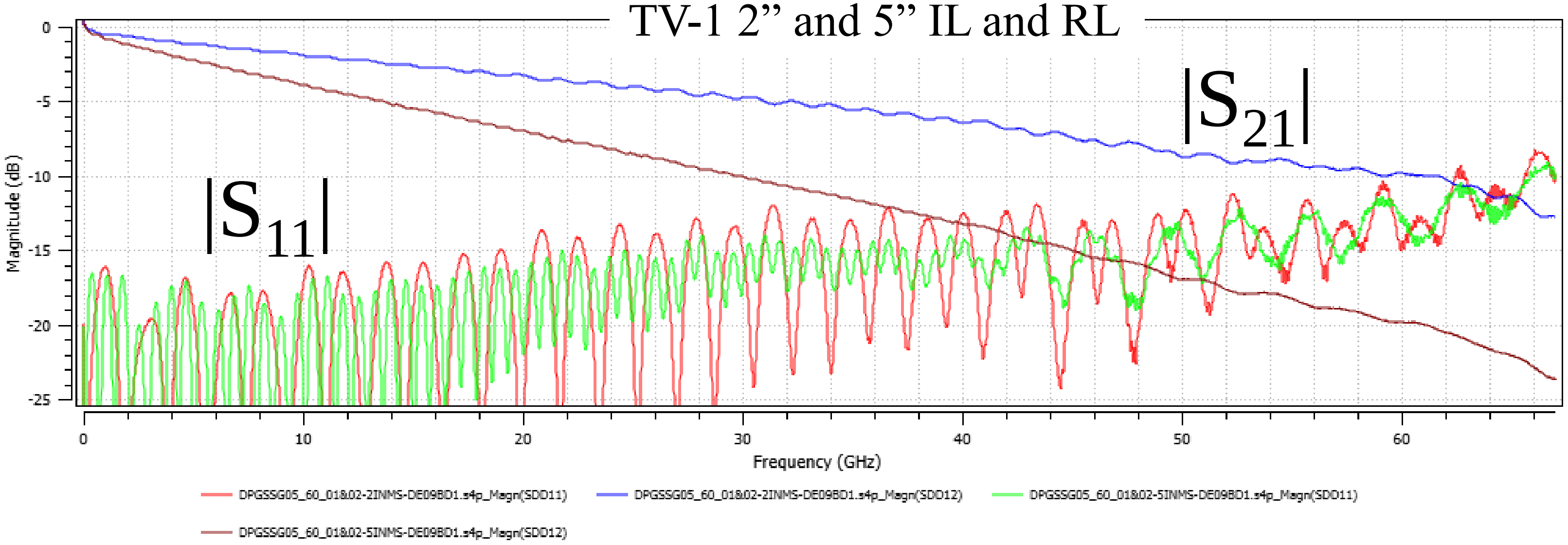


TV-1 2” and 5” TDR



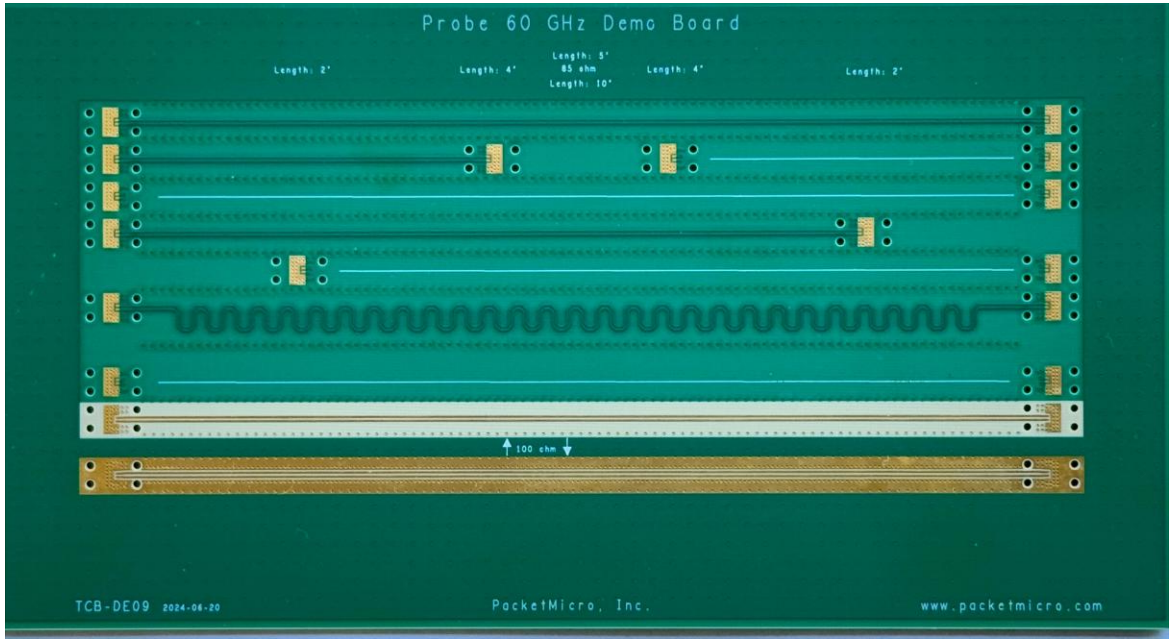
Probe properties:

- 0.5 mm pitch
- GSSG configuration
- 3-mil robust probe tip
- 47-mi Coaxial cable
- 1.85 mm Samtec connector
- Stainless bases

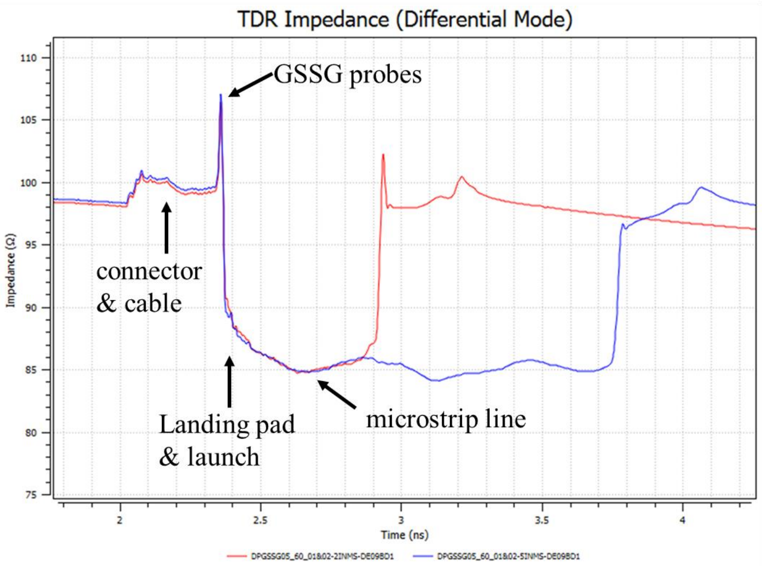


67 GHz Delta-L TV-1

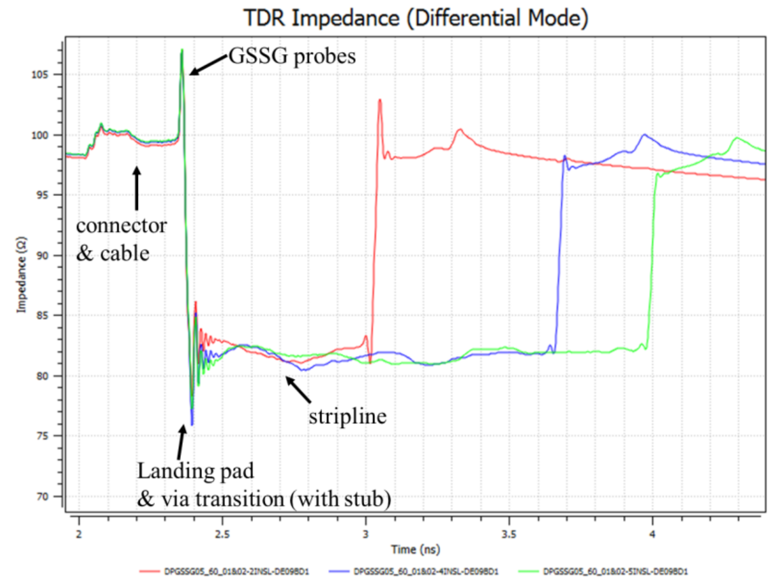
6-layer, Megtron 6, 2”, 4”, 5” µstrip and stripline



Layer No	LAYER DESCRIPTION	Segment	Cu WT(OZ PER SQ FT)	EST THK (MILS)	Differential (85 Ohms+/-10%) LW/LS (MILS)	Calculated Zdiff	Dk @1GHz	Df @1GHz
	SOLDERMASK							
1	TRACE	Cu	0.5 + Plating	1.6	12/5.75	83.45		
		Prepreg	R-5670G (1078x2)	6.68			3.15	0.002
2	GND	Cu	1	1.35	REF	REF		
		Core	R-5775G	11.81			3.45	0.002
3	GND	Cu	1	1.35	REF	REF		
		Prepreg	R-5670G (1080+2116x3)	17.11			3.58	0.002
4	GND	Cu	1	1.35	REF	REF		
		Core	R-5775G	11.81			3.45	0.002
5	TRACE	Cu	1	1.35	10/10	85.69		
		Prepreg	R-5670G (1078x2)	6.43			3.15	0.002
6	GND	Cu	0.5 + Plating	1.6	REF	REF		
	SOLDERMASK							
	Est Board thickness over conductors (mils)			62.44				
	Meg6			mils				

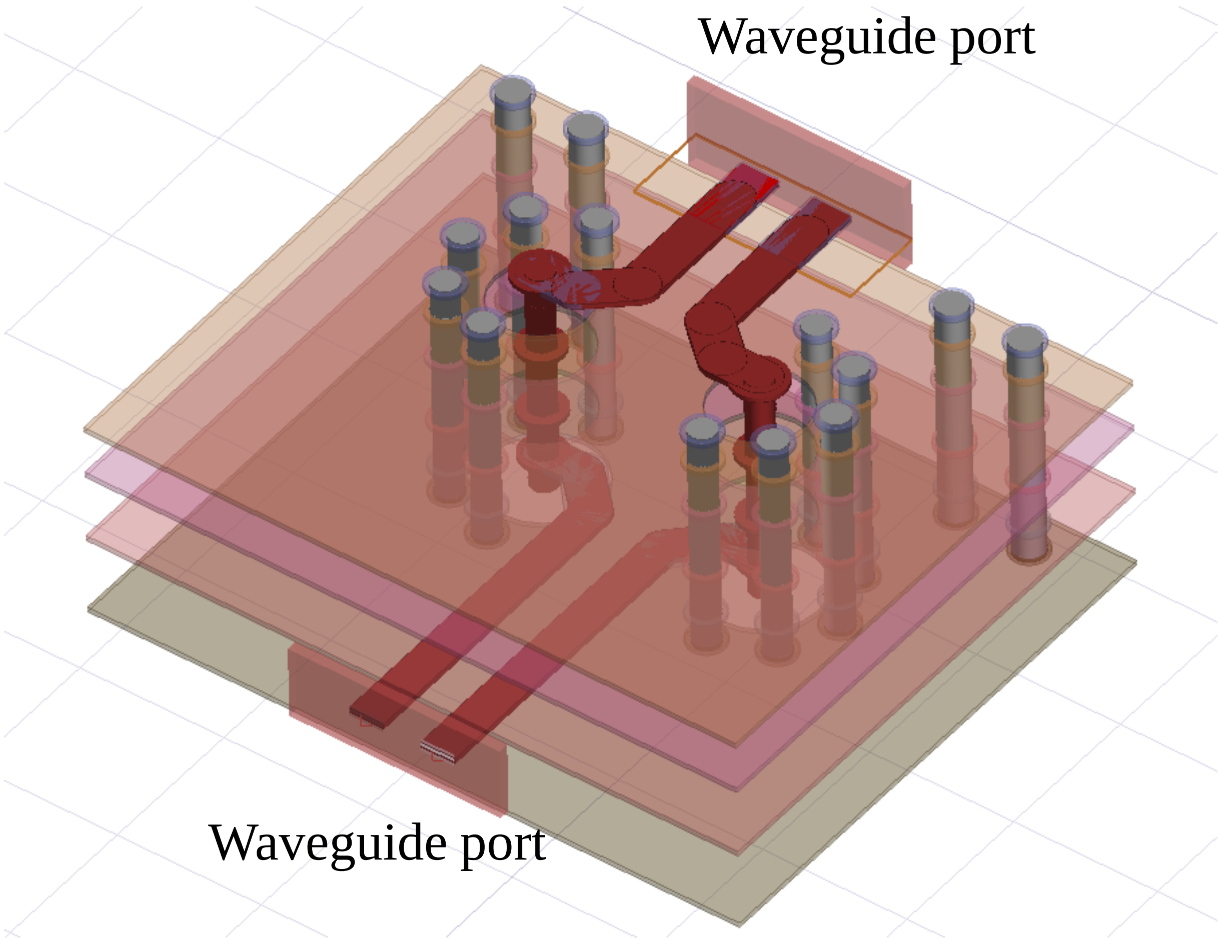


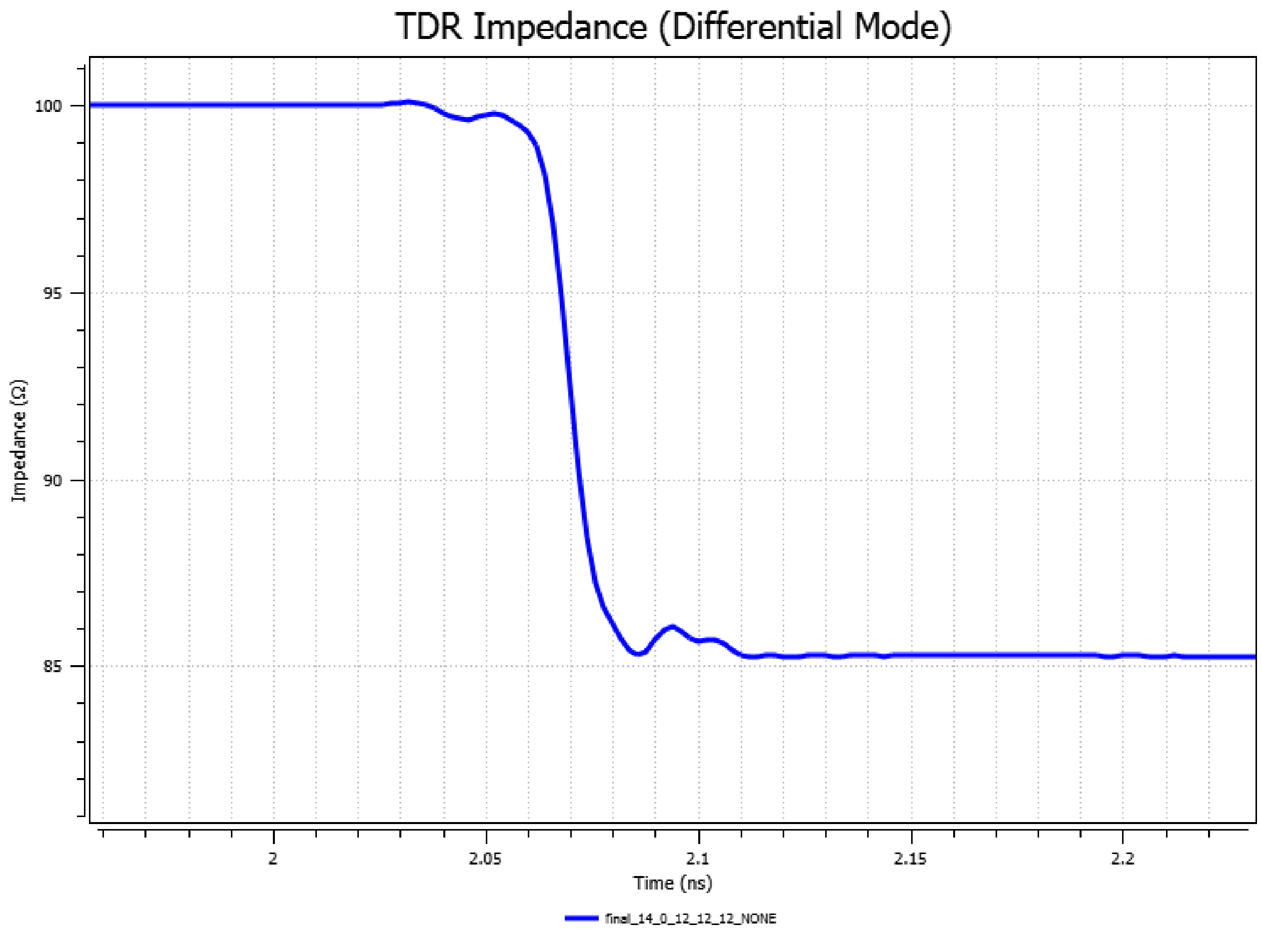
µstrip Layer 1



Stripline Layer 5

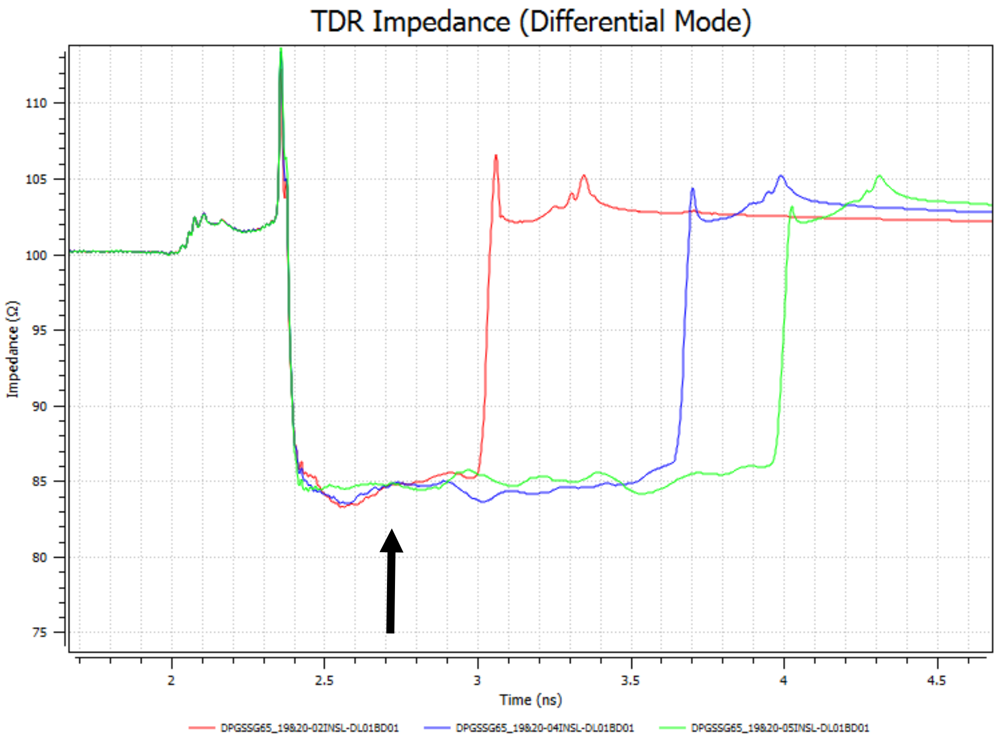
67 GHz Delta-L TV-2 Design & EM Modeling

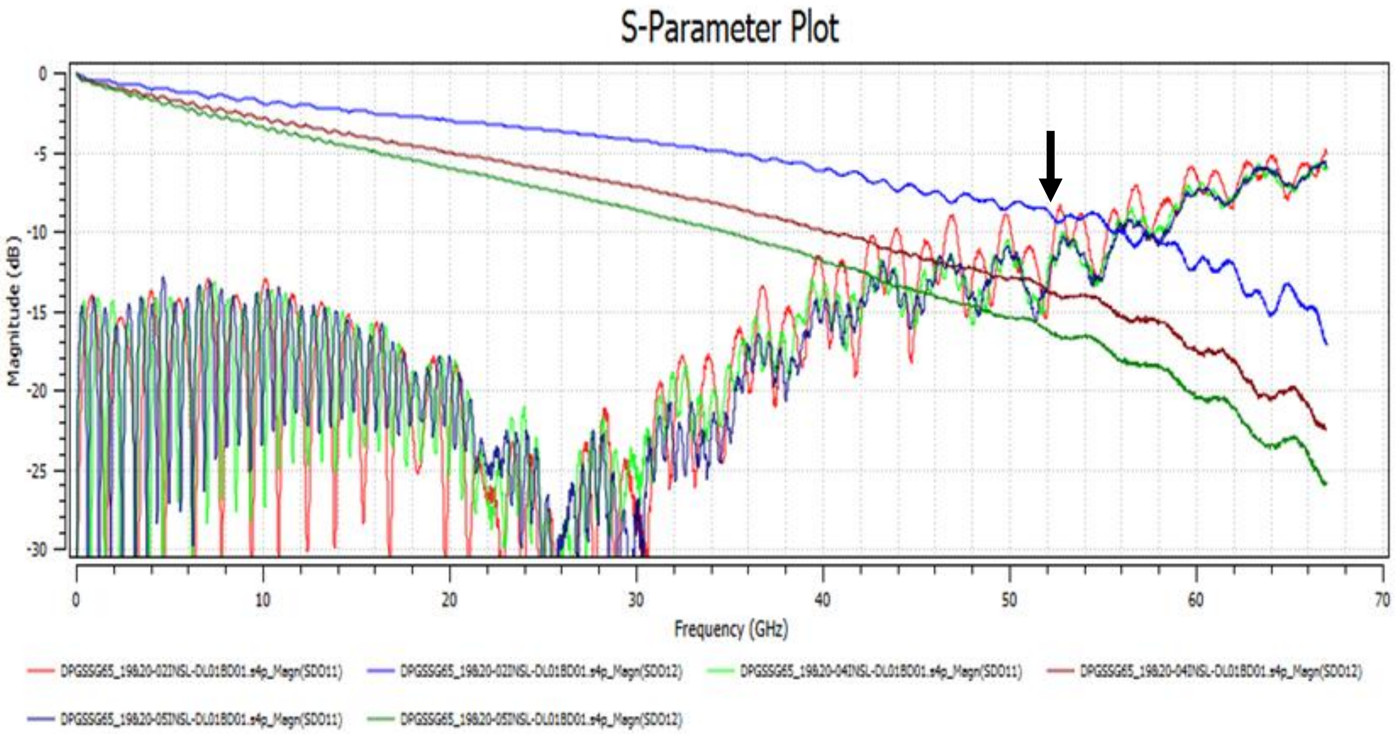




67 GHz Delta-L TV-2 – Measured TDR, RL, IL

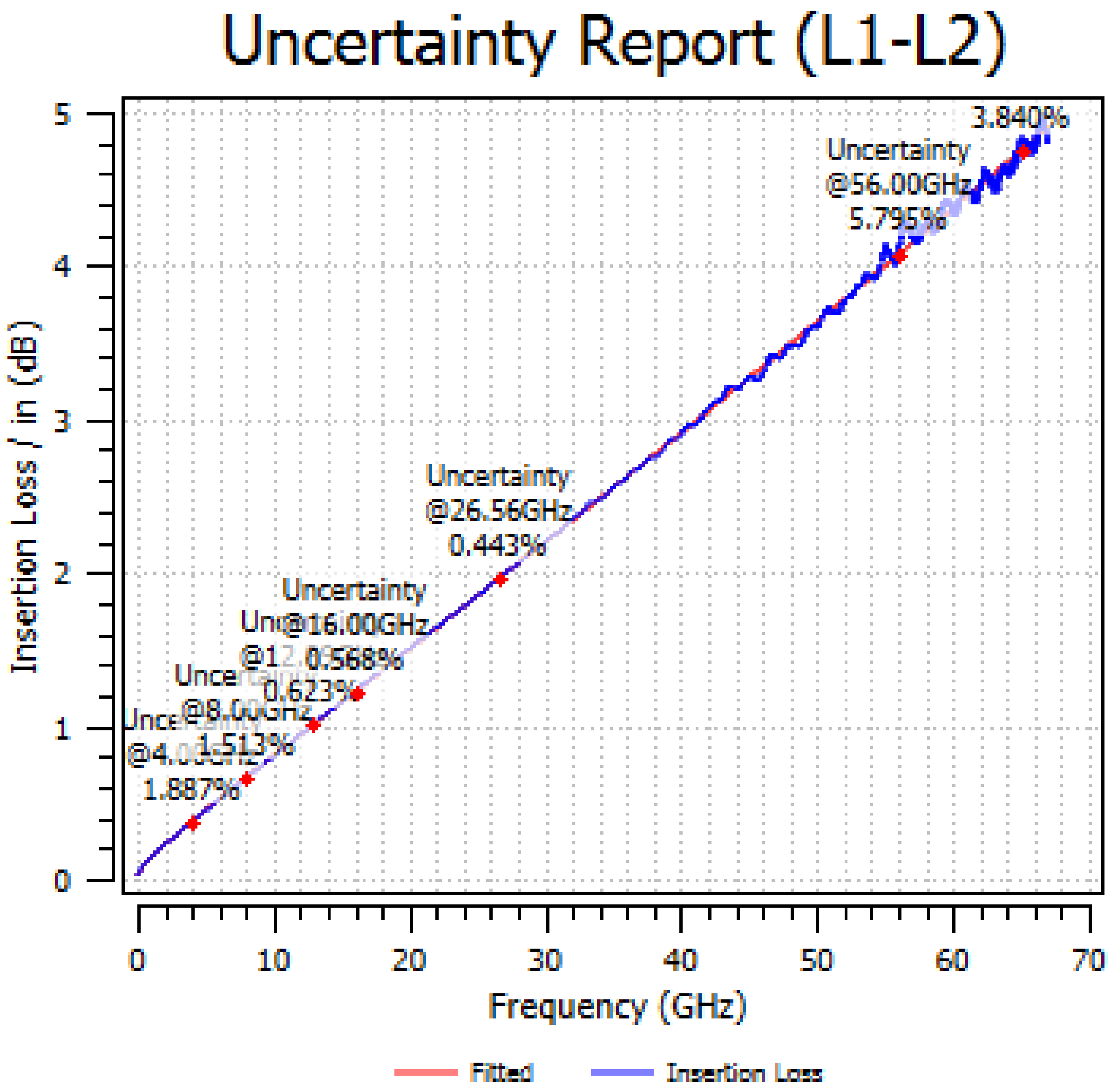
The IL and RL cross at approximately 52 GHz.

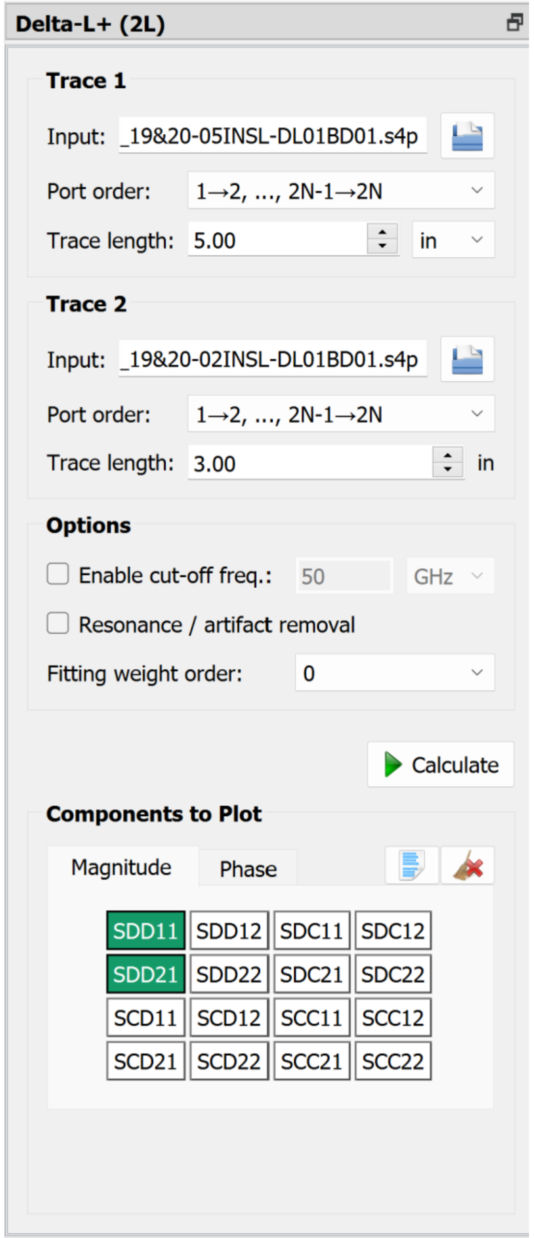




A 2” length for 2X Thru is not necessary, and a shorter length would better satisfy IEEE 370.

67 GHz Delta-L TV-2 – Delta-L Results





Conclusion

Achieving a good outcome for Delta-L to 67 GHz will necessitate:

- Robust handheld probe – achieved with PacketMicro GSSG
- Excellent design using EM simulation to develop the design
  - Probe and footprint optimization – work from Delta-L 4.0 Universal Footprint
  - Via transition design
    - Backdrilling (possibly with air fill, i.e., no plug in the backdrill)
    - Per layer optimization
    - Material/Dk dependent
    - Fabrication/capability dependent
    - Fabrication technology – HDI (Type 4) vs. PTH (Type 3)
- High-quality S-parameter measurements

Next Steps

- Clear Signal Solutions/PacketMicro 6-layer, Megtron 6 TV(s)
  - Any update to Delta-L 4.0 Universal Footprint
  - Via transition optimization for PTH
- Intel higher layer count TV(s)

Some EM Simulation Tools (incomplete)

- EMCoS Studio (MoM)
- Cadence Clarity (TD-FDTD, FD-FEM)
- CST Studio Suite – Dassault Systems (TD-FIT, FD-FEM)
- HFSS – Ansys (FD-FEM)
- EMA3D (TD-FDTD)

Thank you!

Questions?

(May also send Jim Drewniak questions or request for slides
james.drewniak@clearsig.com , put “DesignCon Delta-L slides” in header)